

SF1

Rev: 1.1

Revision History :

1. Ver A: Initial L4S6MG

2. Ver B:

- I. P12 Del Pull-down when no 1394
- II. P14 Modify clock gen enable & bus select CKT
- III. P20 Modify PCI3 routing to DABC & Del AC97 reset CKT
- IV. P21 Add D30 for EZJ1-CDROM
- V. P22 Modify UD2+-, UD3+- NET
- VI. P25 Add COM2 CP8, CP9
- VII. P26 Modify FAN CTRL BJT for 772 to 2907
- VIII. P28 Modify FPMIC NET
- IX. P29 Modify VCCBUS CKT & Del CMF4, RN15
- X. P30 RTL8100C/8110S Co-layout
- XI. P31 Modify VCC3_DUAL, SB_M, SB1.8V, AUX_IVDD CKT
- XII. P32 Modify VCC1.8V, VDDQ, IVDD, DDRVTT CKT
- XIII. P33 ADP3180/RT9247 Co-layout
- XIV. P34 Add LJ2, LSMI1 & Modify EZJ1-CDROM & Modify BATOK CKT

3. Ver C:

- I. Del EZJ1(P11, P21, P34)
- II. Del FANCTL#2, WOL1 and Modify HW temp monitor for TF(P23, P26)
- III. Add Jack-detect circuit(P27, P28)
- IV. Del CNR1(P20)
- V. Del RN18(P14)
- VI. Modify VCC_DUAL circuit For S5(P31)
- VII. Add SR for 661FX and R371 for DDRVTT(P32)
- VIII. Add LAN RCR circuit(P30)
- IX. meet 648/661/660 new 3in1 trace length

4. Ver 1.0: 15-K08-011001

- I. Add LMDN1 & Modify for ALC202A&655(P27)
- II. USB+LUSB(P22)
- III. Add CPU Temp header(P04)
- IV. VGA1/COM3 co-layout(P25)
- V. Add WOL1, WOM1 and FAN_CTRL2(P26)
- VI. Modify IR header(P24)
- VII. Modify VRD for 9.0 + 10.0(P33)


5. Ver 1.1: 15-K08-011101

- I. Modify IO location
- II. Modify for ALC655(P27,P28)
- III. FAN Control Co-layout(P26)
- IV. IEEE1394a Add 4*2 header(P25)
- V. Modify RTL8110S Power(P30)

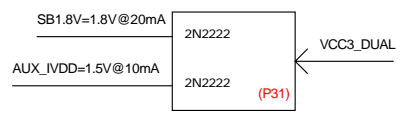
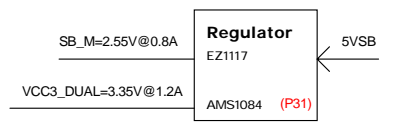
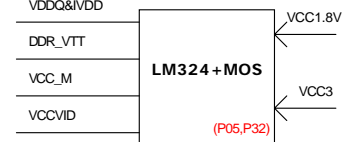
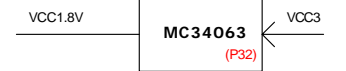
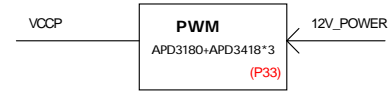
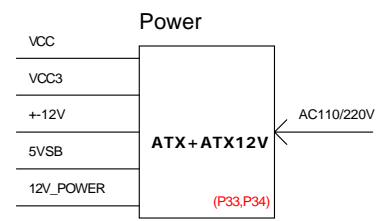
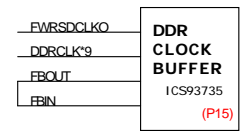
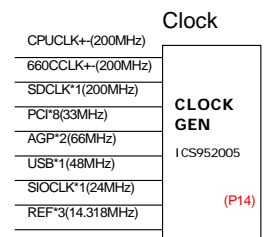
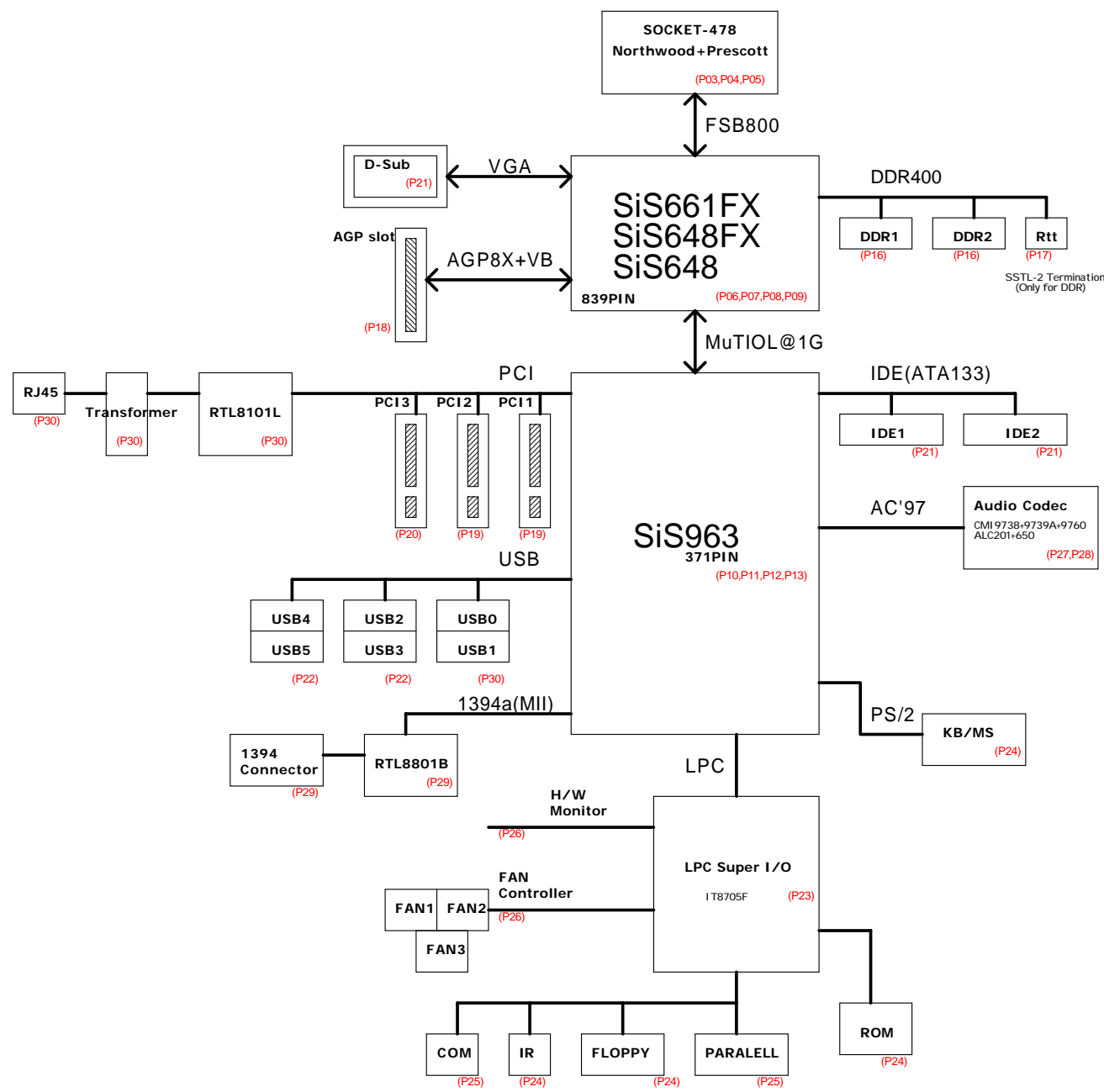
Page Index

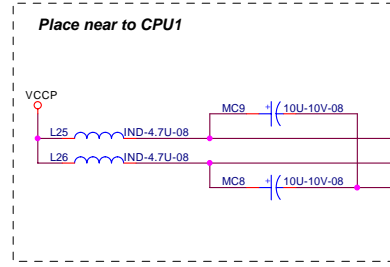
=====

- 01. Cover Sheet
- 02. Block Diagram
- 03. Socket478-1
- 04. Socket478-2
- 05. Decoupling Circuit
- 06. SiS648FX-1 (HOST / AGP)
- 07. SiS648FX-2 (Memory)
- 08. SiS648FX-3 (HyperZip)
- 09. SiS648FX-4 (Power)
- 10. SiS963-1 (PCI / IDE / HyperZip)
- 11. SiS963-2 (Misc. Signals)
- 12. SiS963-3 (USB)
- 13. SiS963-4 (Power)
- 14. Main Clock
- 15. Clock Buffer
- 16. DIMM 1, 2
- 17. DDR Termination
- 18. AGP slot
- 19. PCI 1, 2
- 20. PCI 3 / CNR
- 21. VGA / IDE Connectors
- 22. USB Connector
- 23. ITE8705
- 24. KB/MS/ROM/FDC/IR
- 25. COM 1,2 / LPT
- 26. HM/FAN/RING/LPC
- 27. Audio Codec
- 28. Audio Interface
- 29. IEEE1394 (RTL8801B)
- 30. LAN RTL8100C/8110S
- 31. DUAL 5V, 3V& SB Regulator
- 32. Voltage Regulator
- 33. Vcore Power
- 34. ATX/Panel/RTC

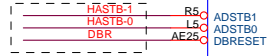
 Elitegroup Computer Systems			
Title SF1/648FX			
Size	Document Number		Rev
Custom	Cover Sheet		1.1
Date:	Tuesday, August 26, 2003	Sheet	1 of 34

System Block Diagram

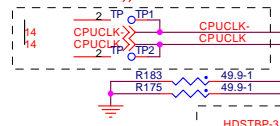




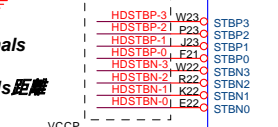
Strobe signals與旁邊trace保持21mils距離



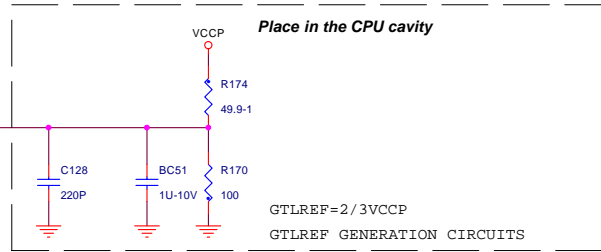
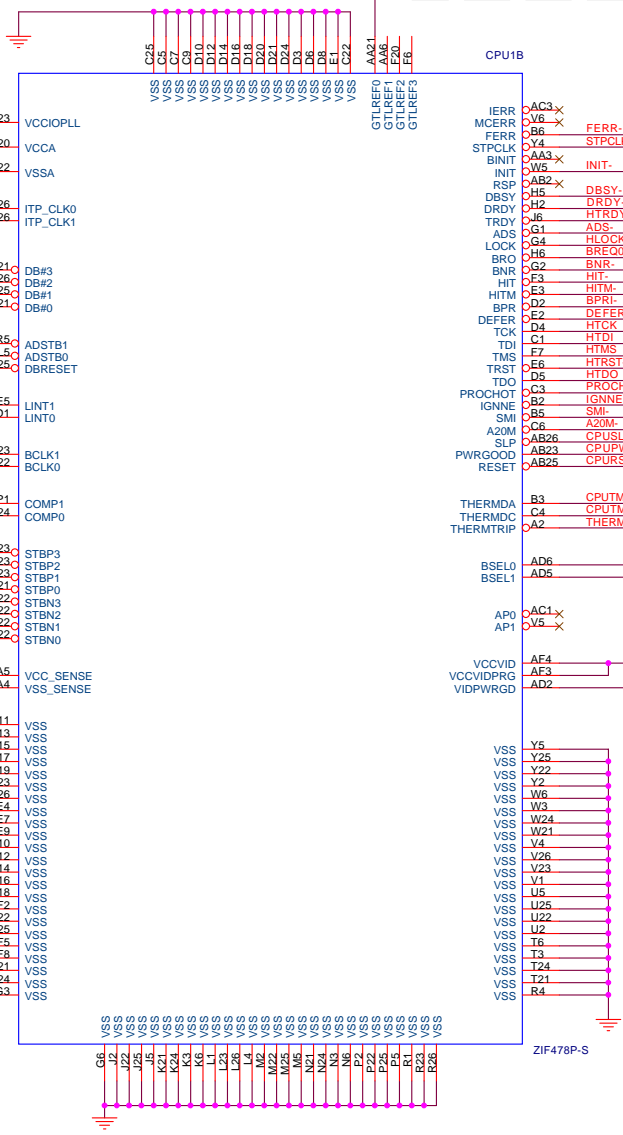
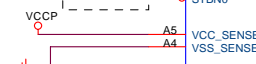
**Differential Clock signals
成雙對稱走線,
並與旁邊trace保持18mils距離**



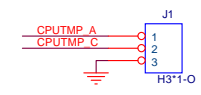
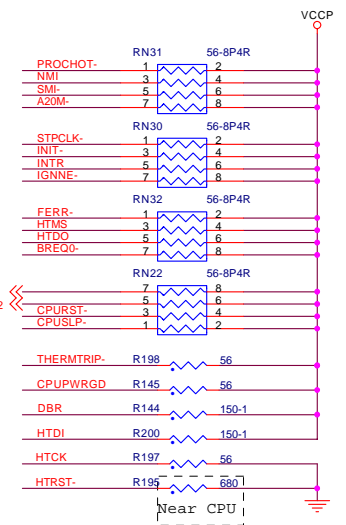
**Differential Strobe signals
成雙對稱走線,
並與旁邊trace保持21mils距離**



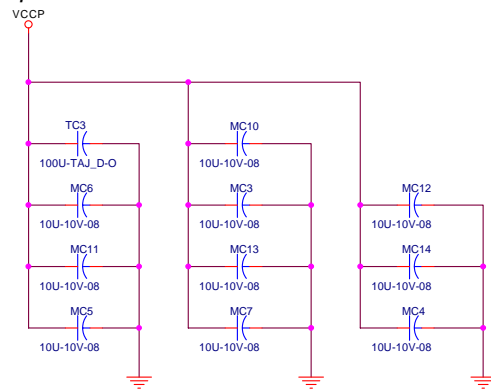
	R175, R183
COMPATIBLE	49.9_1%
OPTIMIZED	61.9_1%



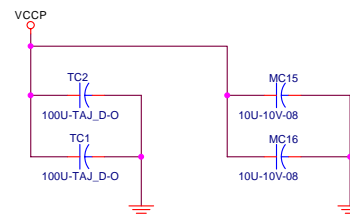
DBI-[0..3] << DBI-[0..3] 6
 HDSTBN-[0..3] << HDSTBN-[0..3] 6
 HDSTBP-[0..3] << HDSTBP-[0..3] 6
 HASTB-[0..1] << HASTB-[0..1] 6



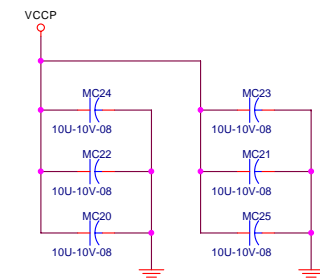
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

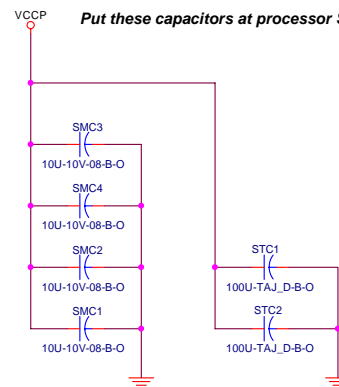


Put these capacitors at processor SOUTH SIDE

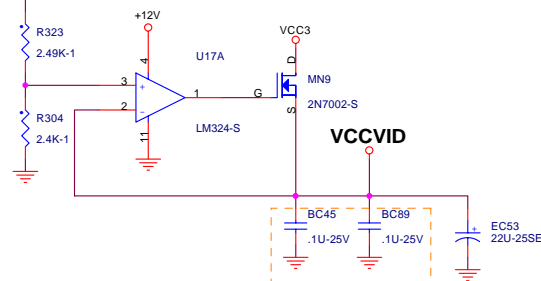


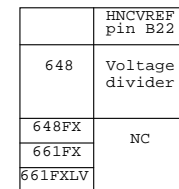
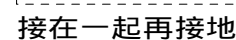
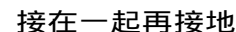
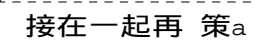
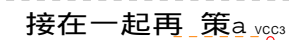
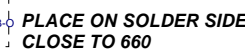
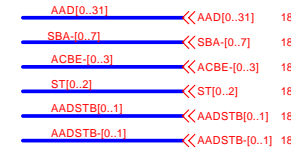
P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

Put these capacitors at processor SOLDER SIDE



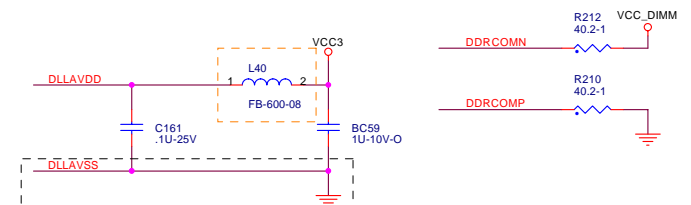
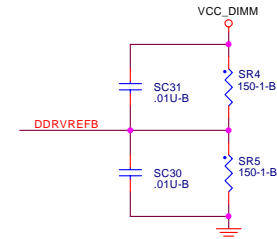
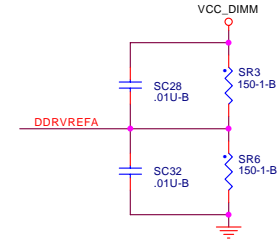
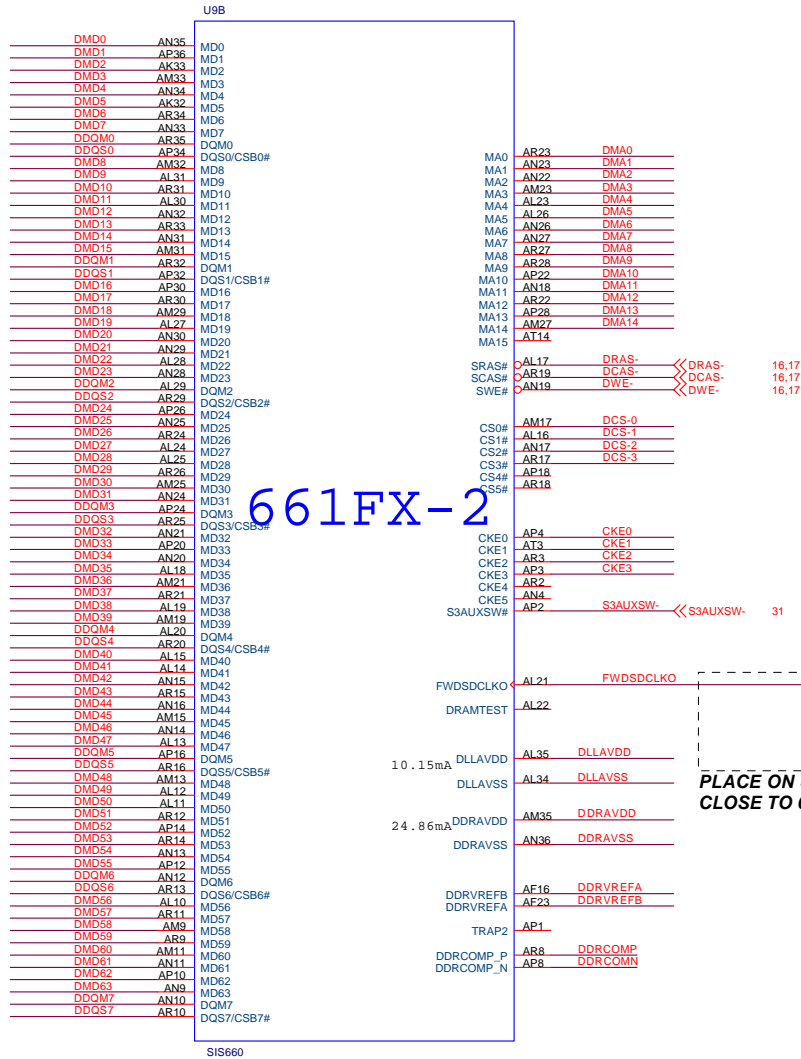
2.5VREF



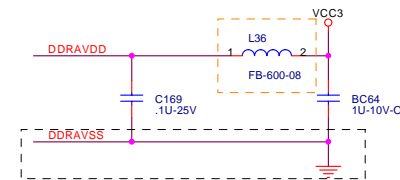


	R143	R133
648	20 1%	110 1%
648FX	14 1%	100 1%
661FX	14 1%	100 1%
661FXLV	14 1%	100 1%

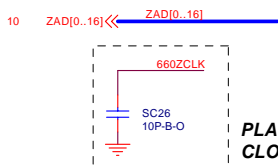
DMD[0..63]	16,17
DDQM[0..7]	16,17
DDQS[0..7]	16,17
DMA[0..14]	16,17
DCS[0..3]	16,17
CKE[0..3]	16



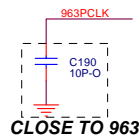
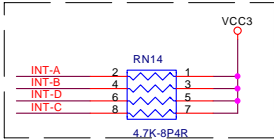
接在一起再接地



接在一起再接地



**PLACE ON SOLDER SIDE
CLOSE TO 660**



19,20,30 CBE[0..3] << CBE[0..3]

8,18,19,20 INT-A << INT-A
18,19,20 INT-B << INT-B
19,20,30 INT-C << INT-C
19,20 INT-D << INT-D

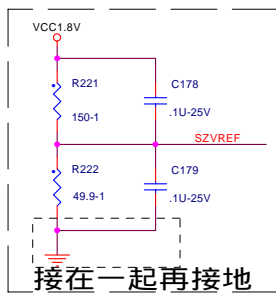
19,20,30 FRAME- << FRAME-
19,20,30 IRDY- << IRDY-
19,20,30 TRDY- << TRDY-
19,20,30 STOP- << STOP-

19,20,30 SERR- << SERR-
19,20,30 PAR << PAR
19,20,30 DEVSEL- << DEVSEL-
19,20 PLOCK- << PLOCK-

14 963PCLK << 963PCLK
18,19,20,21,30 PCIRST- << PCIRST-
23 SIOPCIRST- << SIOPCIRST-
8 NBPCIRST- << NBPCIRST-

14 963ZCLK << 963ZCLK
8 ZSTB0 << ZSTB0
8 ZSTB0 << ZSTB0
8 ZSTB1 << ZSTB1
8 ZSTB1 << ZSTB1

8 ZUREQ << ZUREQ
8 ZDREQ << ZDREQ



接在一起再接地

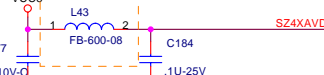
SVDDZCMP << SVDDZCMP
SZCMP_N << SZCMP_N
SZCMP_P << SZCMP_P
SVSSZCMP << SVSSZCMP
SZ1XAVDD << SZ1XAVDD
SZ1XAVSS << SZ1XAVSS
SZ4XAVDD << SZ4XAVDD
SZ4XAVSS << SZ4XAVSS
SZVREF << SZVREF
ZAD16 << ZAD16

8 ZAD[0..16] << ZAD[0..16]

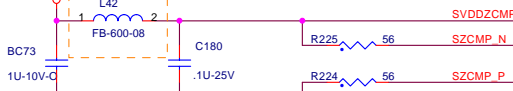
Analog Power supplies of Transzip function for 963 Chip.



接在一起再接地



接在一起再接地



接在一起再接地

U11A

PCI

IDE

963-1

HyperZip

10mA IDEAVDD IDEAVSS

ICHRDYA << ICHRDYA
IDREQA << IDREQA
IIRQA << IIRQA
CBLIDA << CBLIDA
IIOA# << IIOA#
IIOWA# << IIOWA#
IDACKA# << IDACKA#

IDSAA2 << IDSAA2
IDSAA1 << IDSAA1
IDSAA0 << IDSAA0

IDCSA1# << IDCSA1#
IDCSA0# << IDCSA0#

ICHRDYB << ICHRDYB
IDREOB << IDREOB
IIOB# << IIOB#
CBLIDB << CBLIDB

IIOB# << IIOB#
IIOWB# << IIOWB#
IDACKB# << IDACKB#

IDSAB2 << IDSAB2
IDSAB1 << IDSAB1
IDSAB0 << IDSAB0

IDCSB1# << IDCSB1#
IDCSB0# << IDCSB0#

IDEDA0 << IDEDA0
IDA1 << IDEDA1
IDA2 << IDEDA2
IDA3 << IDEDA3
IDA4 << IDEDA4
IDA5 << IDEDA5
IDA6 << IDEDA6
IDA7 << IDEDA7
IDA8 << IDEDA8
IDA9 << IDEDA9
IDA10 << IDEDA10
IDA11 << IDEDA11
IDA12 << IDEDA12
IDA13 << IDEDA13
IDA14 << IDEDA14
IDA15 << IDEDA15

IDB0 << IDEDB0
IDB1 << IDEDB1
IDB2 << IDEDB2
IDB3 << IDEDB3
IDB4 << IDEDB4
IDB5 << IDEDB5
IDB6 << IDEDB6
IDB7 << IDEDB7
IDB8 << IDEDB8
IDB9 << IDEDB9
IDB10 << IDEDB10
IDB11 << IDEDB11
IDB12 << IDEDB12
IDB13 << IDEDB13
IDB14 << IDEDB14
IDB15 << IDEDB15

SIS963

Elitegroup Computer Systems

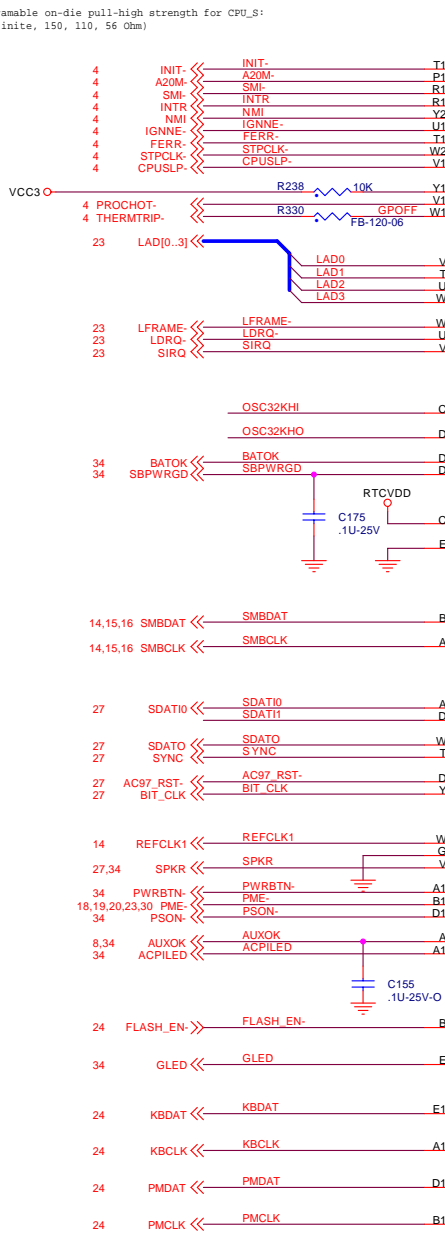
SF1/648FX

Document Number

SIS963-1 (PCI / IDE)

Friday, July 11, 2003

Programable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)



CPU_S

APIC

LPC

RTC

GPIO

AC97

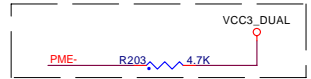
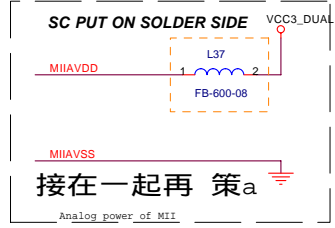
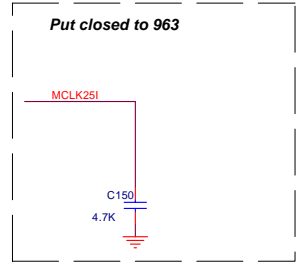
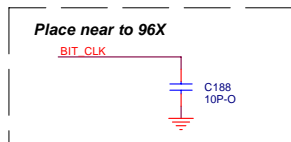
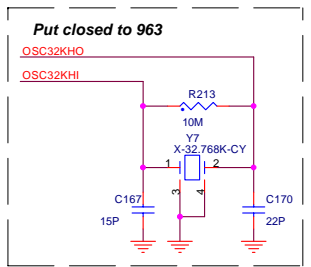
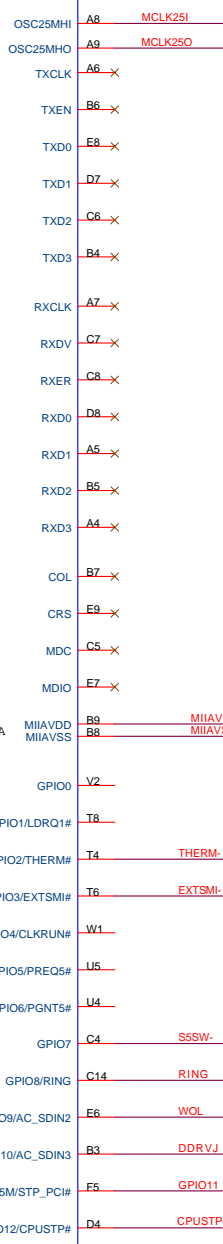
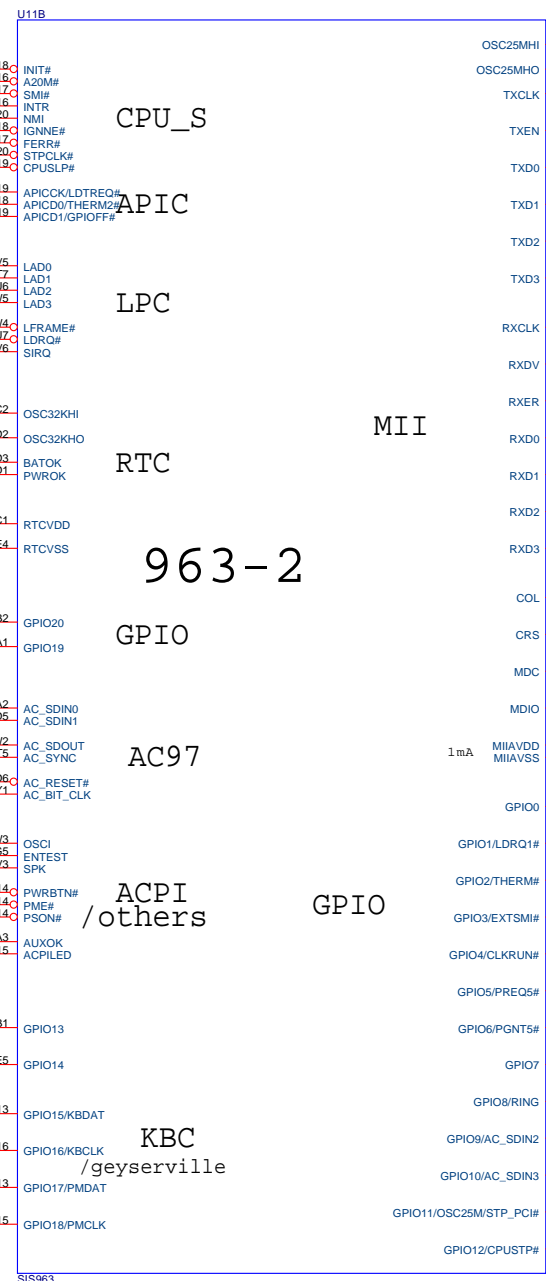
ACPI /others

KBC /geyserville

MII

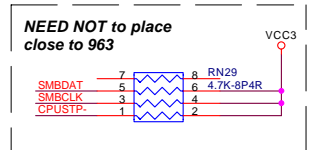
963-2

GPIO

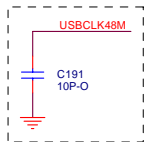


NEED NOT to place close to 963

NEED NOT to place close to 963

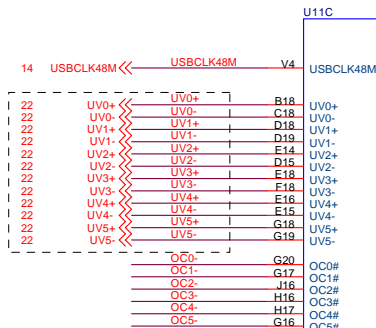


	0	1
GPIO7	W 1394PHY	W/O 1394PHY
GPIO11	W/O S3	W S3



CLOSE TO 963

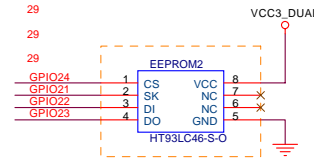
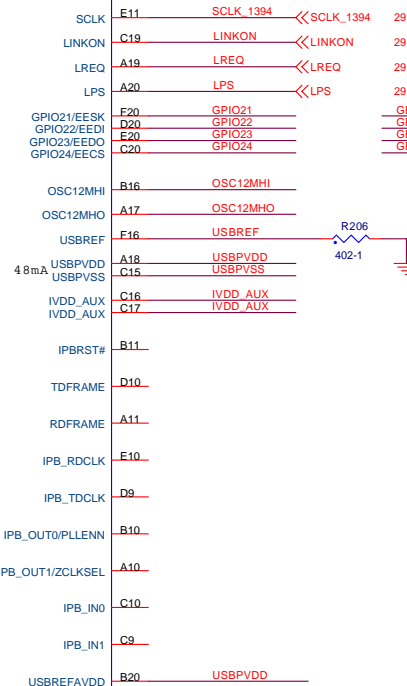
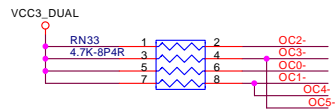
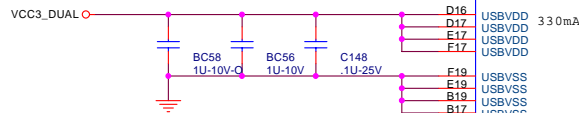
Differential signals
成雙 纜呢挂u



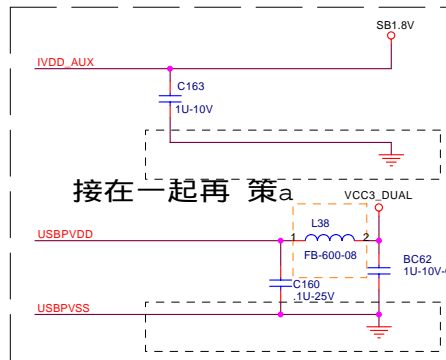
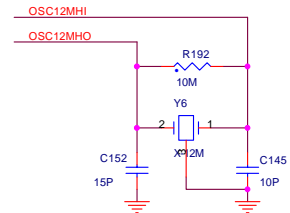
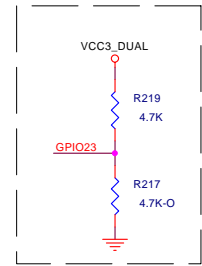
USB

963-3

1394



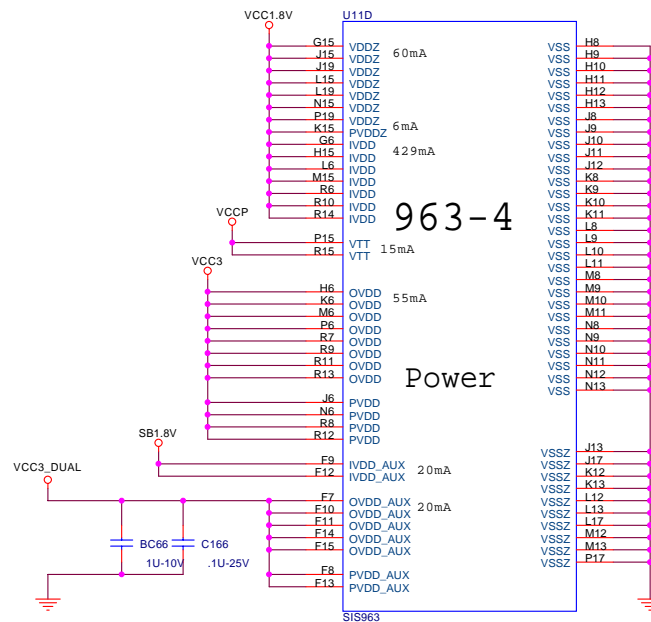
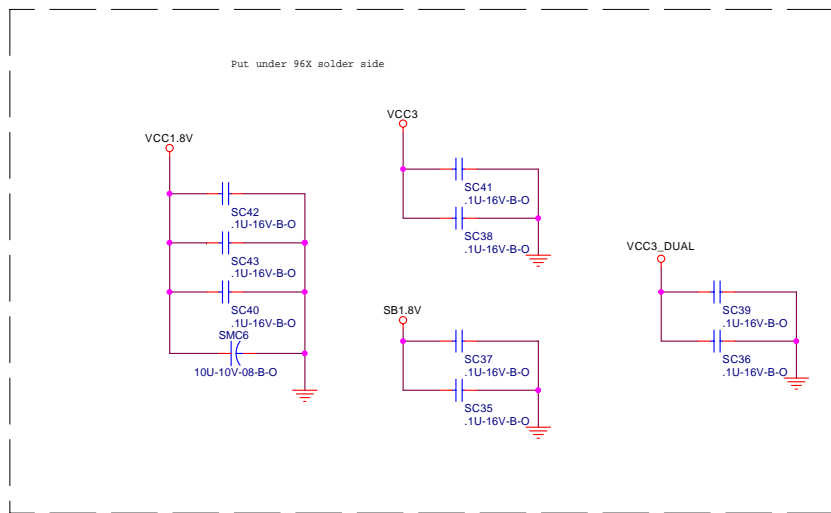
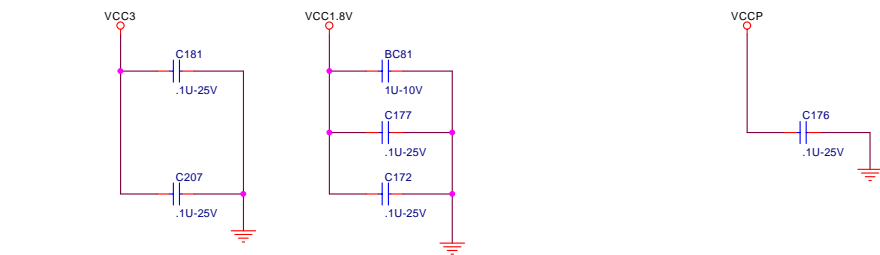
EEDO	High	Low
1394	Enable	Disable



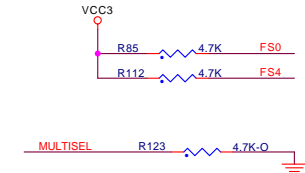
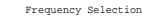
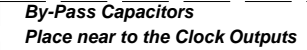
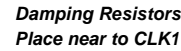
接在一起再 策a

接在一起再 策a

	0	1	Default	
SPKR(LPC_addr mapping)	disable	enable	R169 un-stuff	yes
SYN(PCICLK PLL)	enable	disable	NONE	yes
OC2-(SB_debug mode)	enable	disable	R171 un-stuff	NO
SDAT(Trap from)	PCI AD	ROM	R170 stuff	yes



PLACE TO EVERY POWER PIN



SIS660 CLOCK									
F54	F53	F52	F51	F50	CPU (MHz)	SDRAM (MHz)	AGPCLK (MHz)	PCICLK (MHz)	zCLK (MHz)
1	0	0	0	0	100.20	100.20	66.80	33.40	133.60
1	0	0	0	0	100.20	133.60	66.80	33.40	133.60
1	0	0	0	0	100.20	200.40	66.80	33.40	133.60
1	0	0	1	1	100.20	167.00	66.80	33.40	133.60
1	0	1	0	0	133.60	100.20	66.80	33.40	133.60
1	0	1	0	1	133.60	133.60	66.80	33.40	133.60
1	0	1	1	0	133.60	200.40	66.80	33.40	133.60
1	0	1	1	1	133.60	167.00	66.80	33.40	133.60
1	1	1	1	0	200.50	100.03	66.68	33.34	133.37
1	1	1	1	0	200.50	133.37	66.68	33.34	133.37
1	1	1	1	0	200.50	200.50	66.68	33.34	133.37
1	1	1	1	1	200.50	160.04	66.68	33.34	133.37
1	1	1	0	0	0	166.70	100.03	66.68	33.40
1	1	1	0	0	1	166.70	133.36	66.80	33.40
1	1	1	0	1	1	166.70	166.68	66.68	33.34
1	1	1	0	1	1	166.70	166.70	66.68	33.34

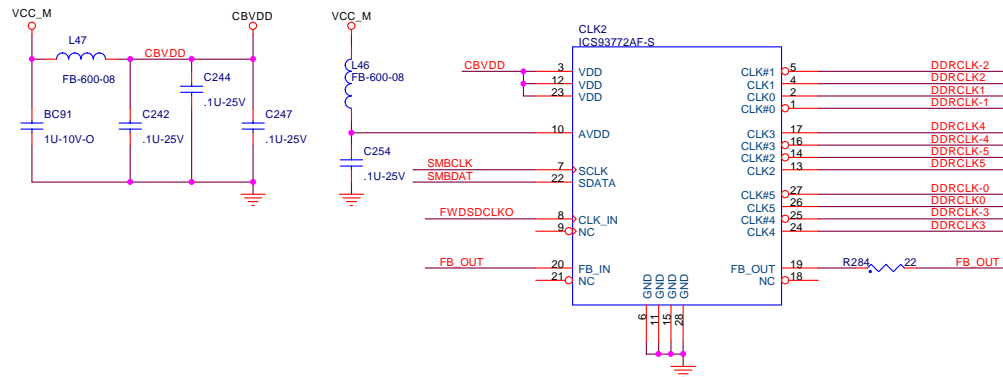
ECS Elitegroup Computer Systems

Title			
SF1/648FX			
Size	Document Number		Rev
Custom	<i>Main Clock</i>		1.1
Date:	Friday, July 11, 2003	Sheet	14 of 34

Change CLK2 footprint
Del BC90, R272, R273,
C255, C257, C239, C243,
C248, EC45

Clock Buffer (DDR)

By-Pass Capacitors
Place near to the Clock Buffer



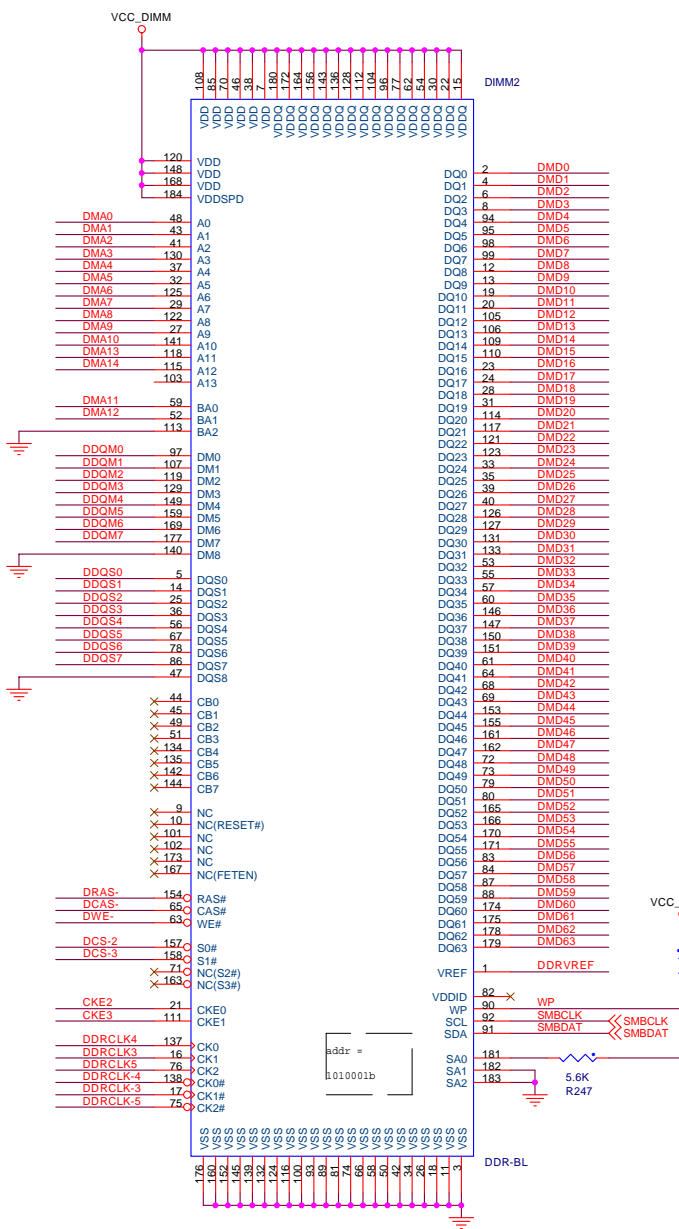
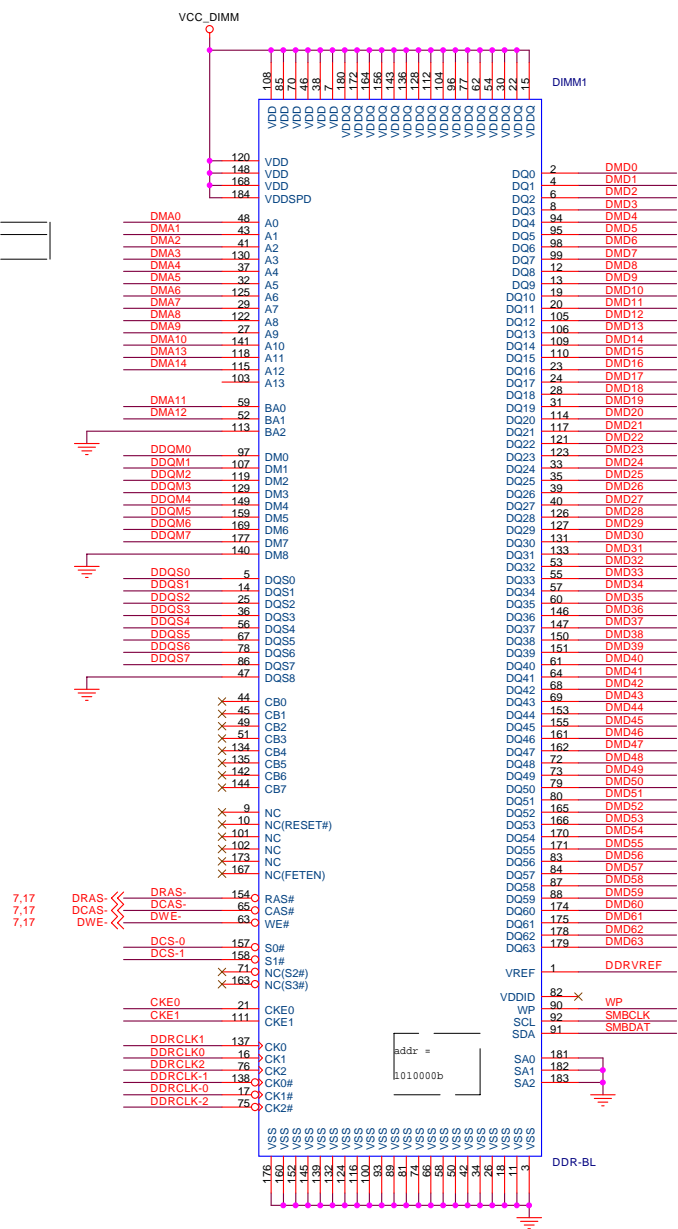
NOTE:

VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

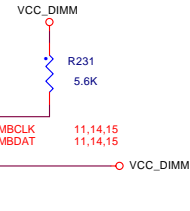
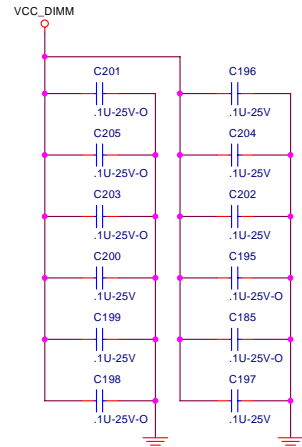
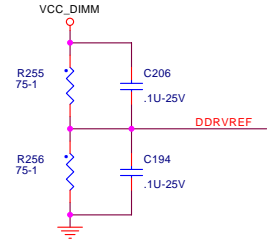
VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

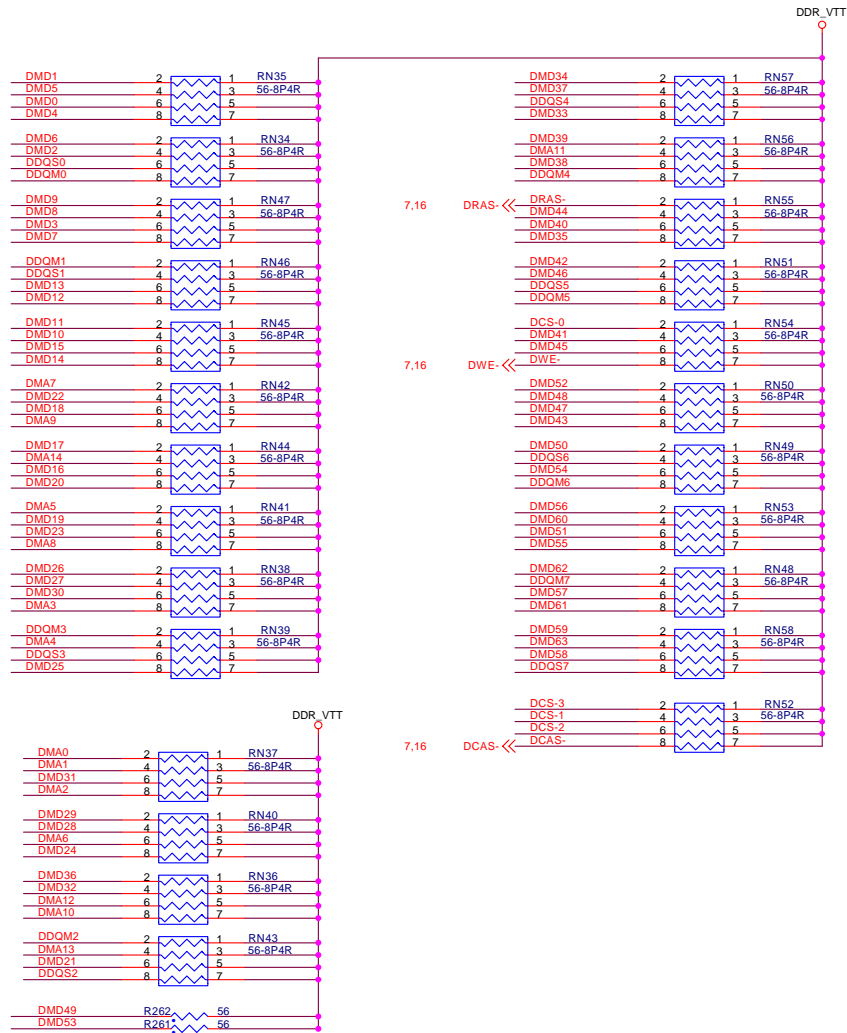


- DMD[0..63] << DMD[0..63] 7,17
- DMA[0..14] << DMA[0..14] 7,17
- DDQM[0..7] << DDQM[0..7] 7,17
- DDQS[0..7] << DDQS[0..7] 7,17
- DCS[0..3] << DCS[0..3] 7,17
- CKE[0..3] << CEK[0..3] 7,17
- DDRCLK[0..5] << DDRCLK[0..5] 15
- DDRCLK[0..5] << DDRCLK[0..5] 15



DMD[0..63]	↔ DMD[0..63]	7, 16
DMA[0..14]	↔ DMA[0..14]	7, 16
DDQM[0..7]	↔ DDQM[0..7]	7, 16
DDQS[0..7]	↔ DDQS[0..7]	7, 16
DCS-[0..3]	↔ DCS-[0..3]	7, 16

SDR		R _{in}	DDR	R _{in}	R _{tt}
MD/DQM (/DQS)	LV-CMOS	0/10/-	STTL-2	1.0	83
MA/Control	LV-CMOS	1.0	STTL-2	0	33
CS	LV-CMOS	0	STTL-2	0	47
CKE	DD 3.3V		DD 2.5V		



DDR_VTT

C237
.1U-25V

C233
.1U-25V

C229
.1U-25V

C225
.1U-25V

C236
.1U-25V

C232
.1U-25V

C228
.1U-25V

C224
.1U-25V

C235
.1U-25V

C231
.1U-25V

C227
.1U-25V

C223
.1U-25V

C234
.1U-25V

C230
.1U-25V

C226
.1U-25V

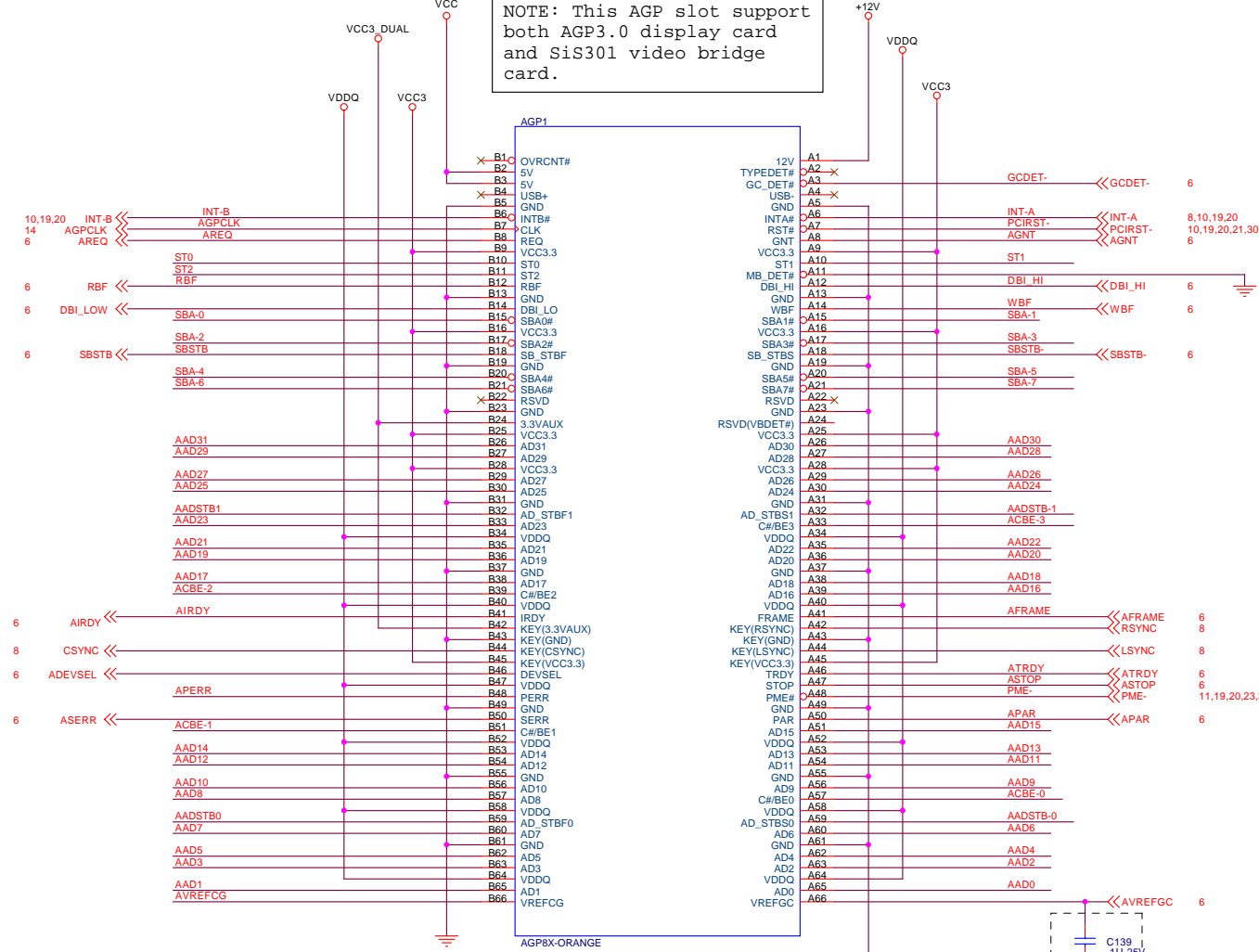
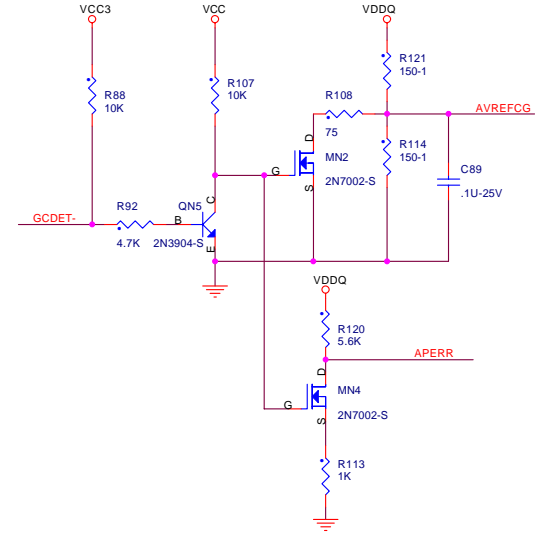
C222
.1U-25V

NOTE: This AGP slot support both AGP3.0 display card and Sis301 video bridge card.

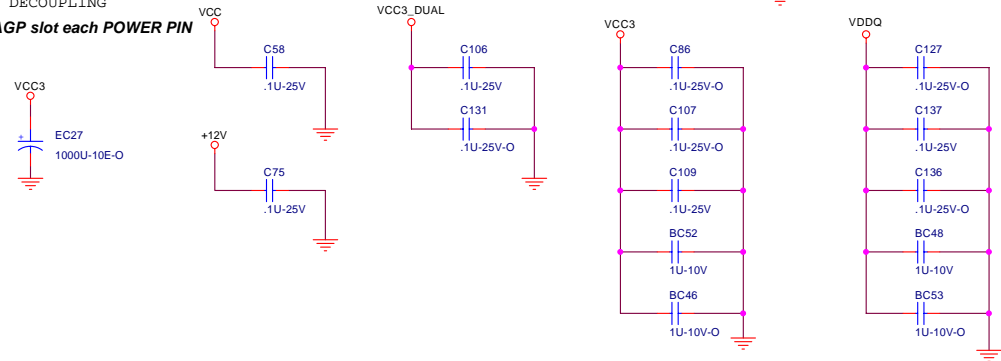
Differential Strobe signals
成雙對稱走線，
並與旁邊trace保持18mils距離

6	SBA-[0..7]	6	SBA-[0..7]
6	ST[0..2]	6	ST[0..2]
6	ACBE-[0..3]	6	ACBE-[0..3]
6	AAD[0..31]	6	AAD[0..31]
6	AADSTB[0..1]	6	AADSTB[0..1]
6	AADSTB-[0..1]	6	AADSTB-[0..1]

GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0

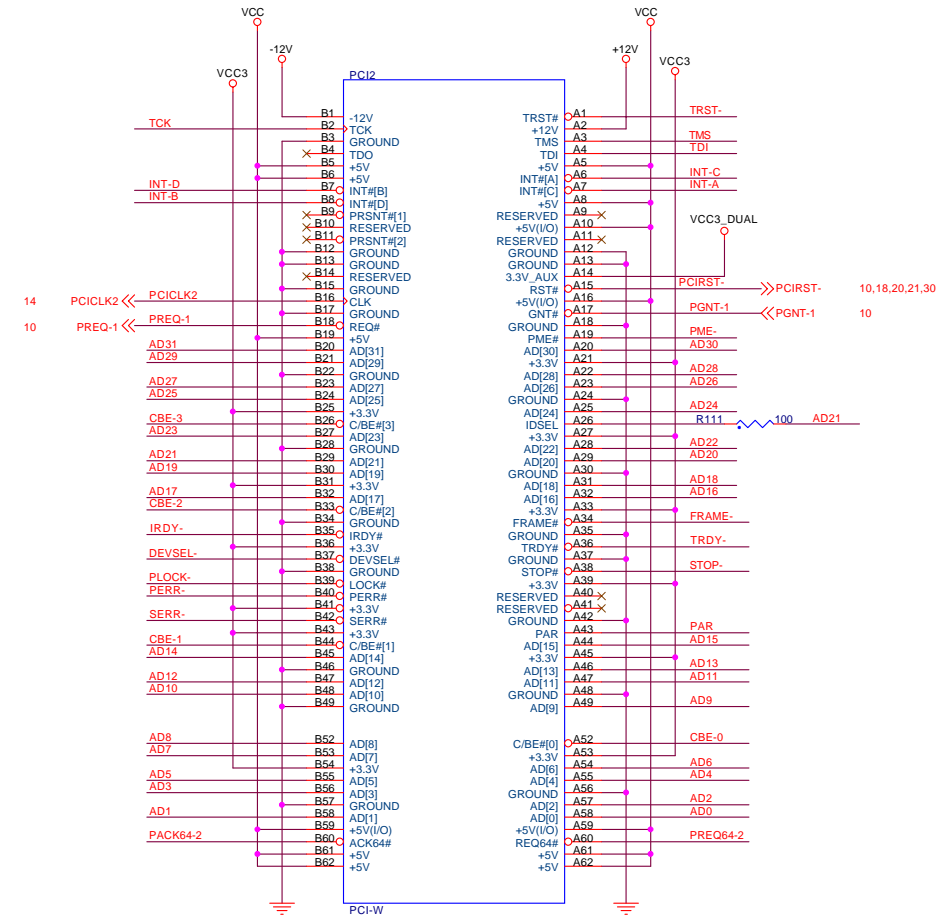
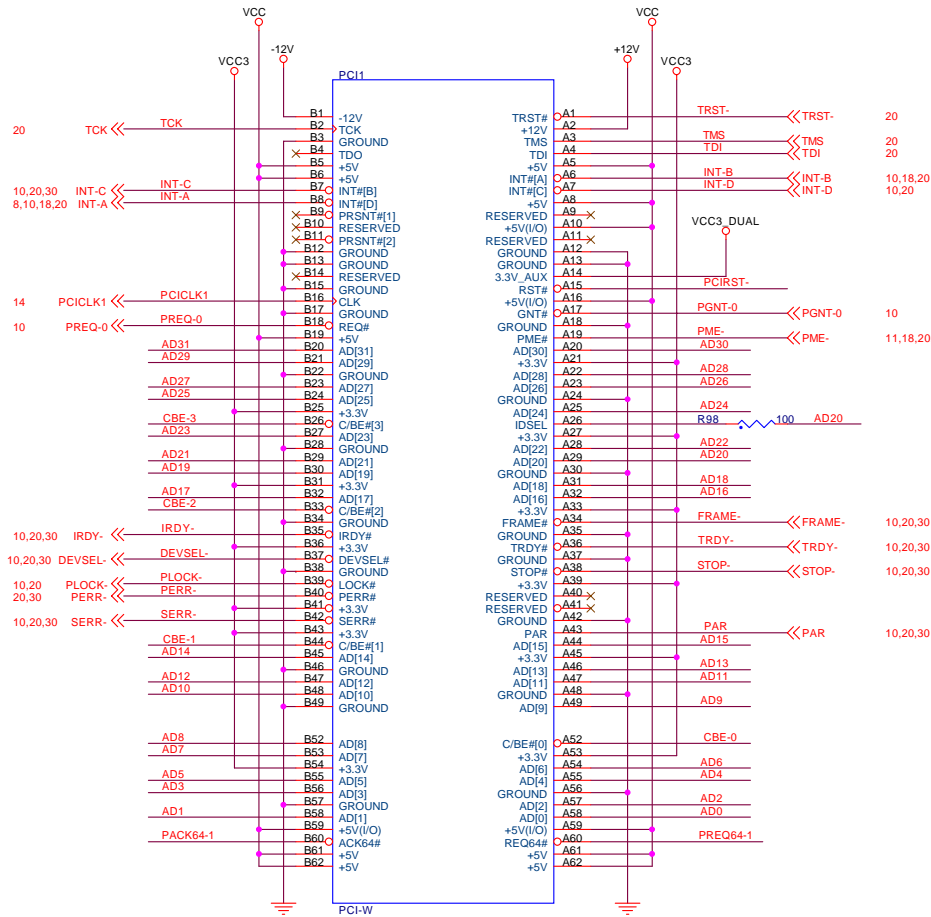


AGP CONNECTOR DECOUPLING
put CAP close to AGP slot each POWER PIN



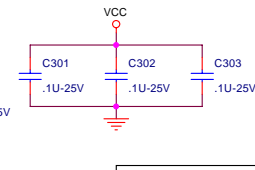
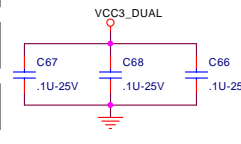
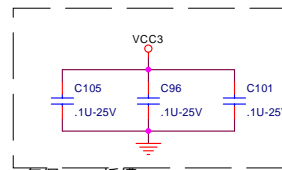
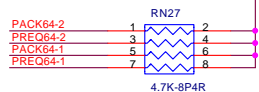
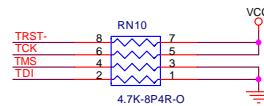
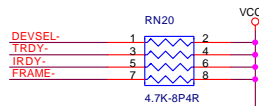
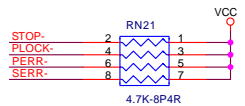
PCI Slot 1 & 2

10,20,30 CBE-[0..3] << CBE-[0..3]
10,20,30 AD[0..31] << AD[0..31]

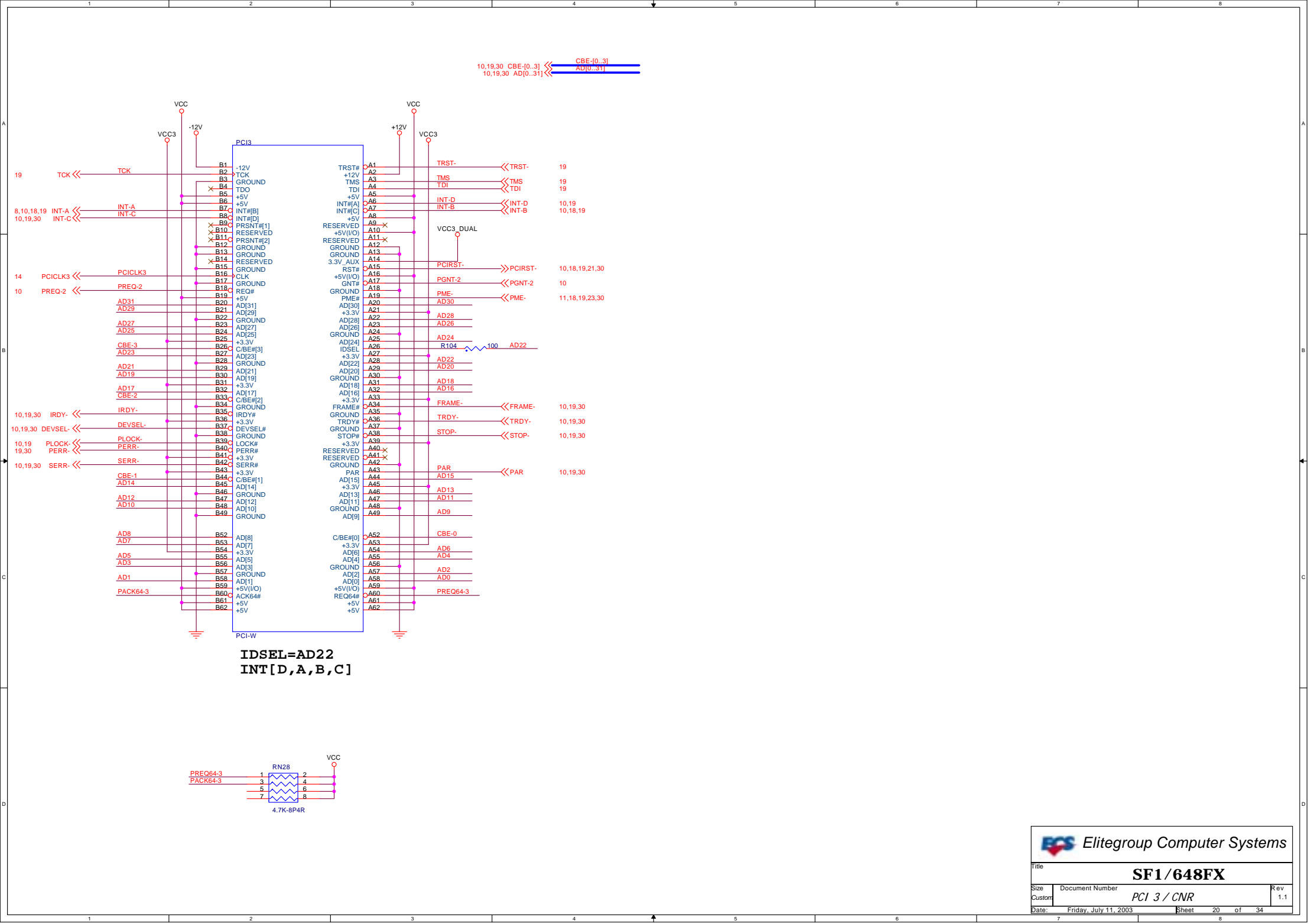


IDSEL=AD20
INT[B,C,D,A]

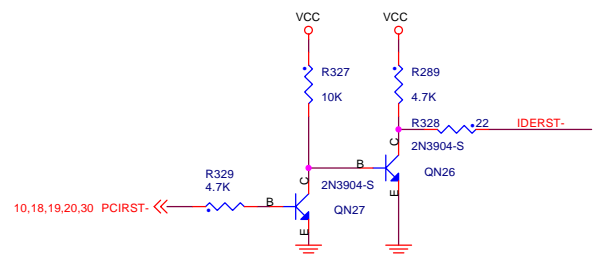
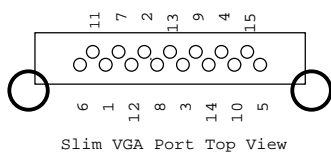
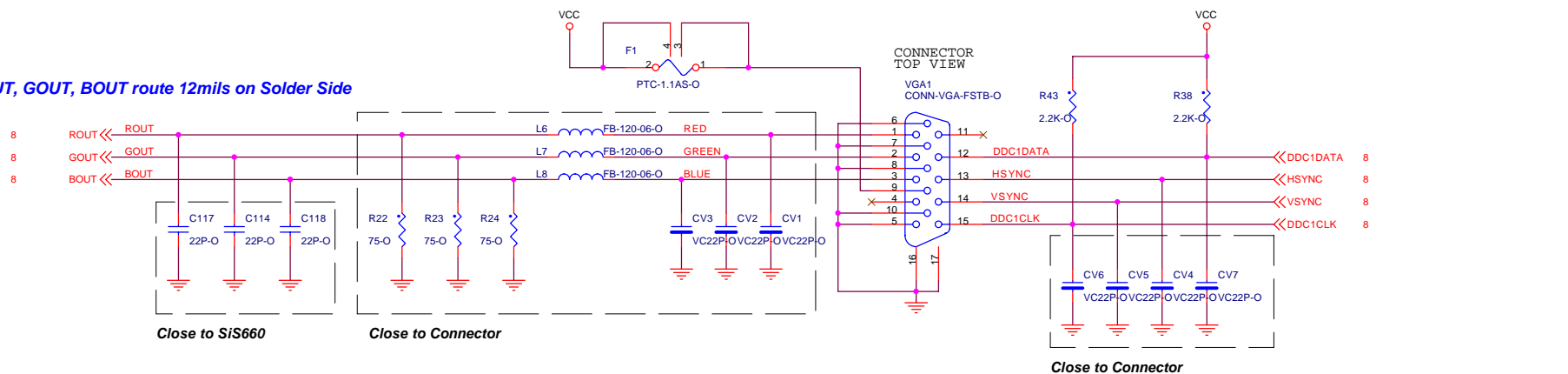
IDSEL=AD21
INT[C,D,A,B]



每個 PCI 插槽 pin A33
各放一顆

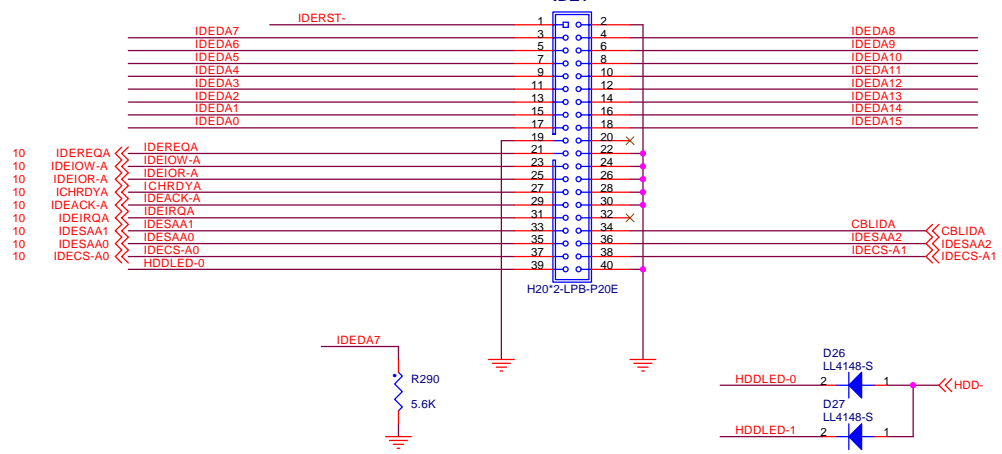


ROUT, GOUT, BOUT route 12mils on Solder Side



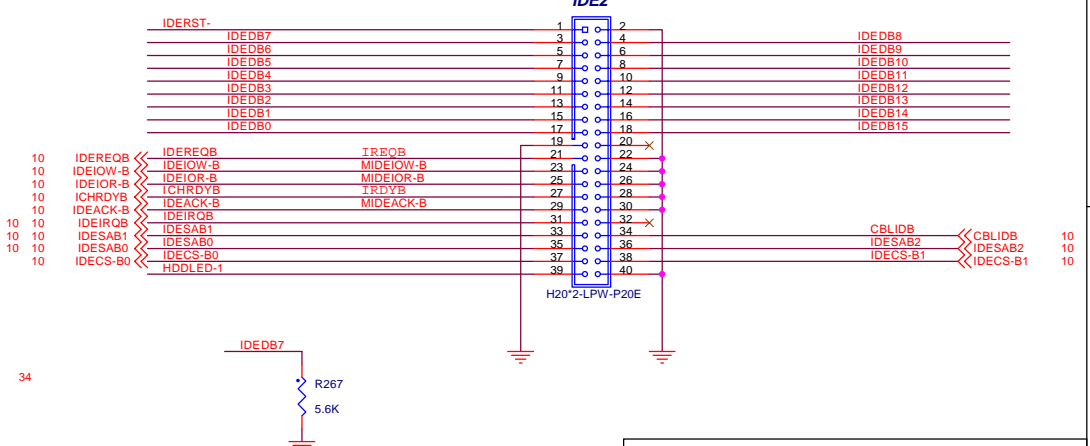
10 IDEDA[0..15] << IDEDA[0..15]

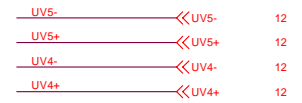
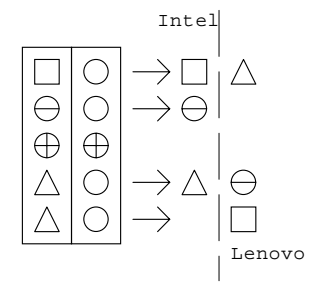
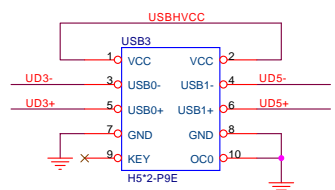
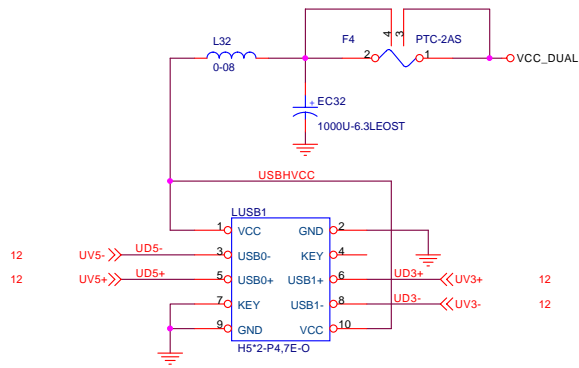
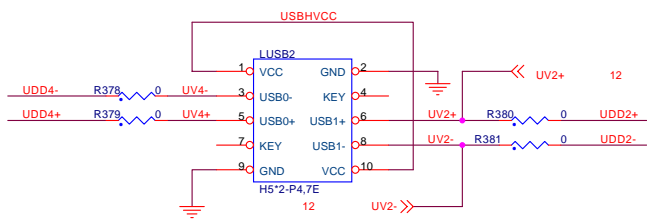
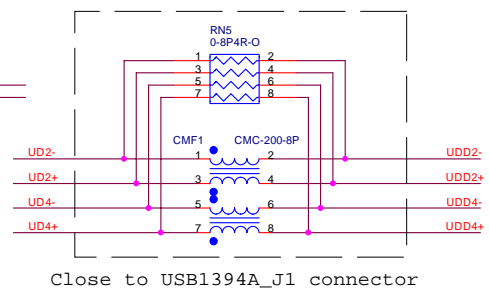
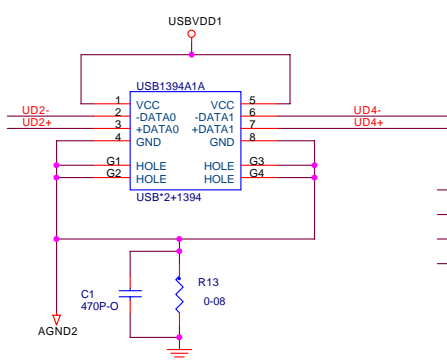
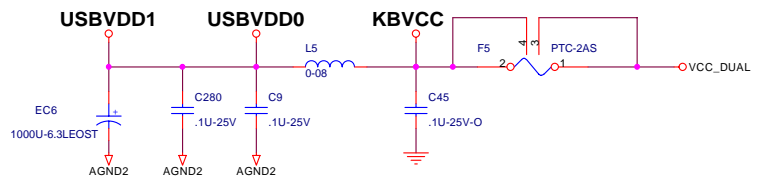
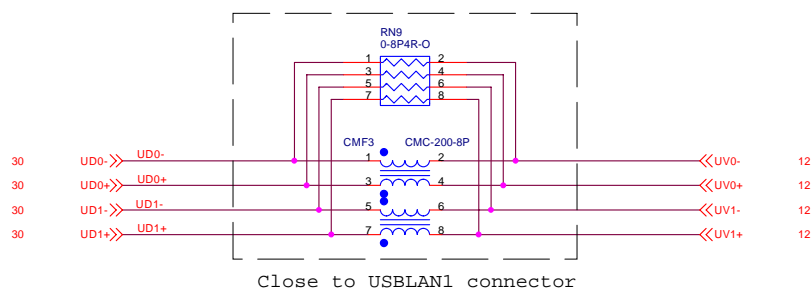
PRIMARY IDE1

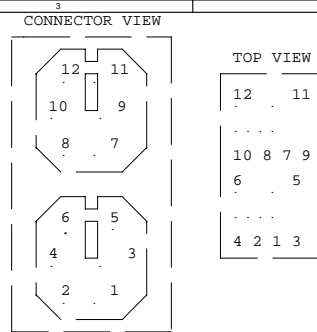


10 IDEDB[0..15] << IDEDB[0..15]

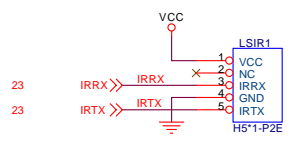
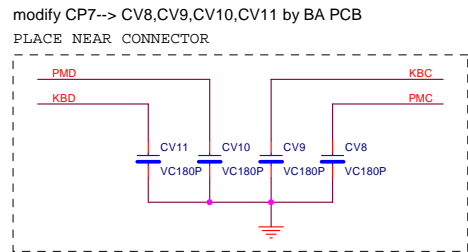
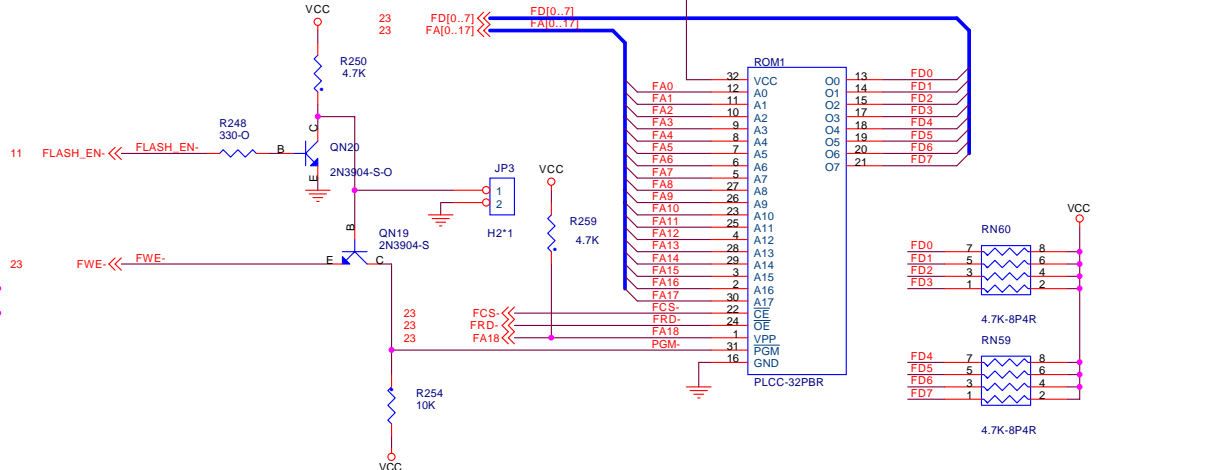
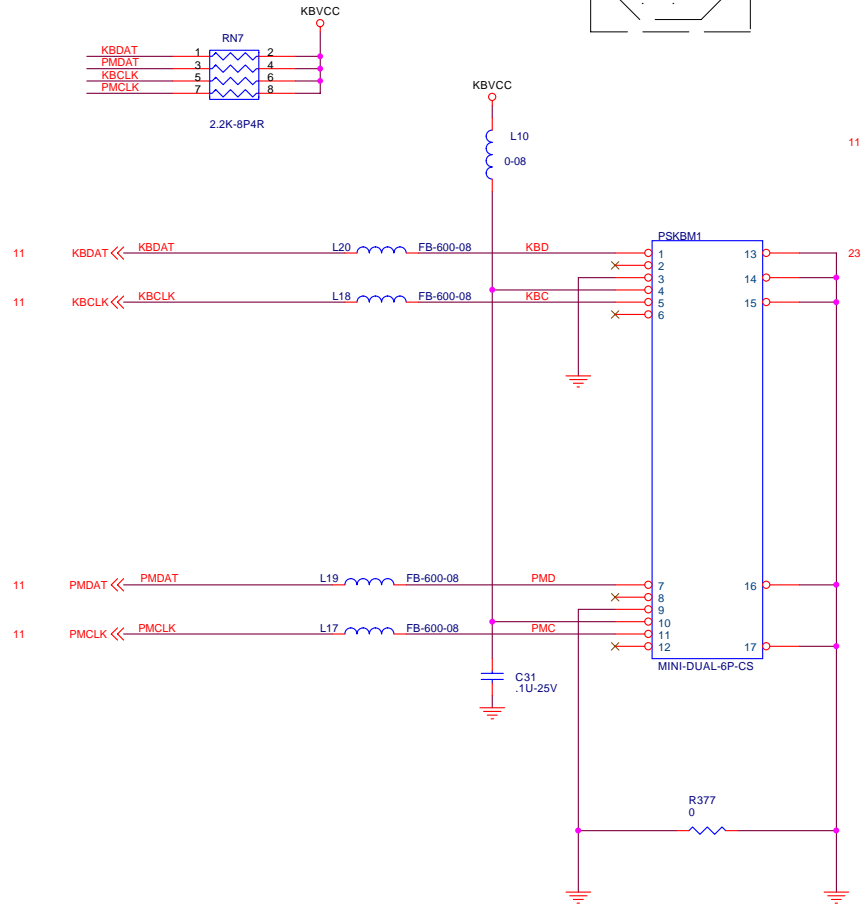
SECONDARY IDE2



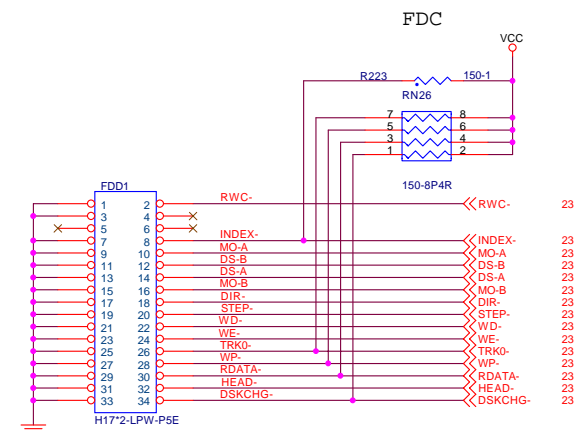




JP3	BIOS PROTECT
OPEN	DISABLE
SHORT	ENABLE

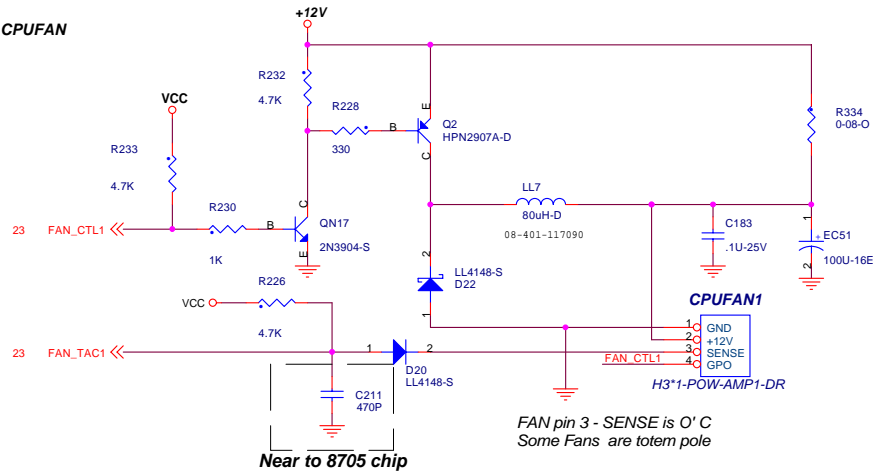


IR CONNECTOR

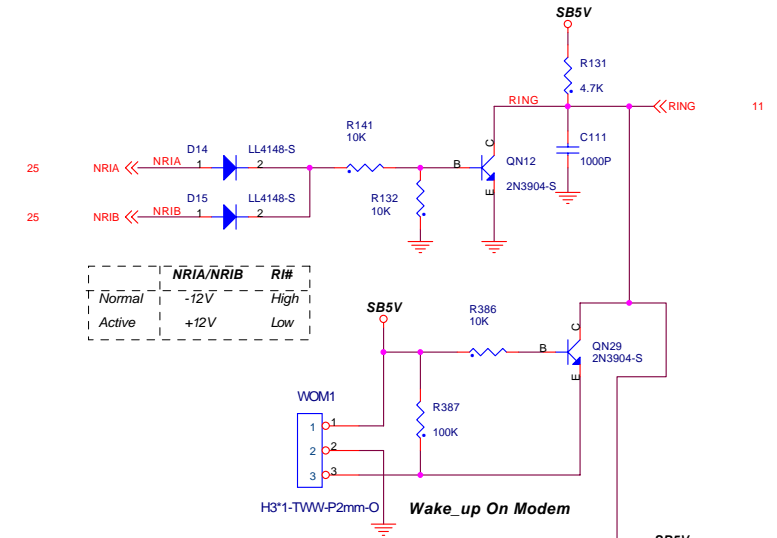
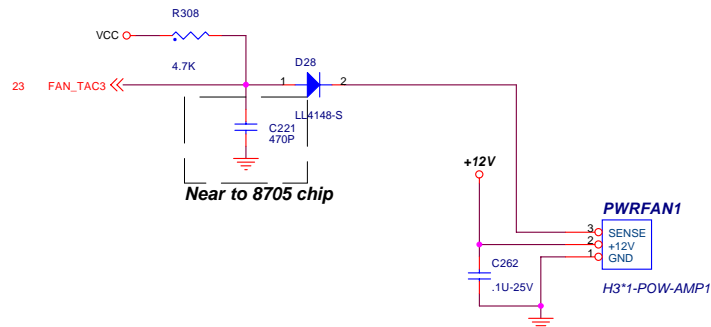
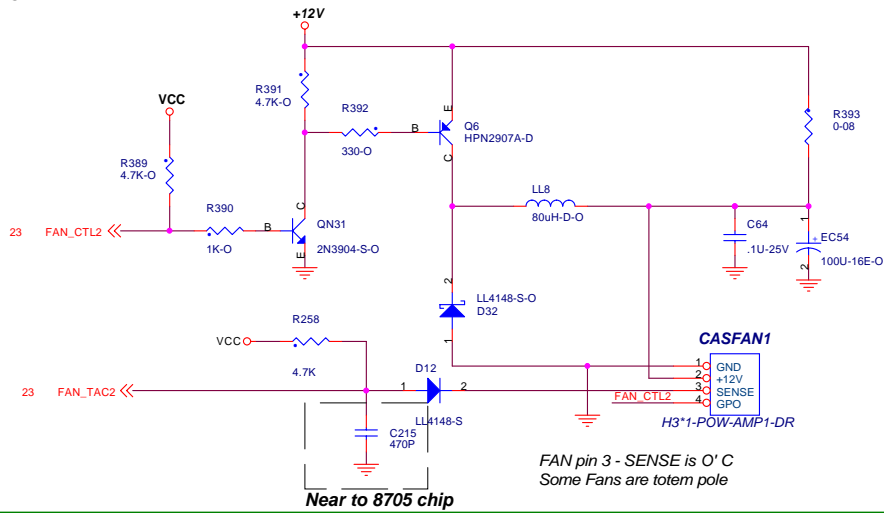


Layout :
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

CPUFAN

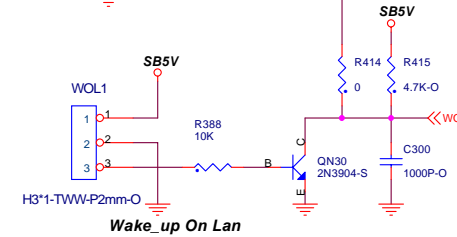
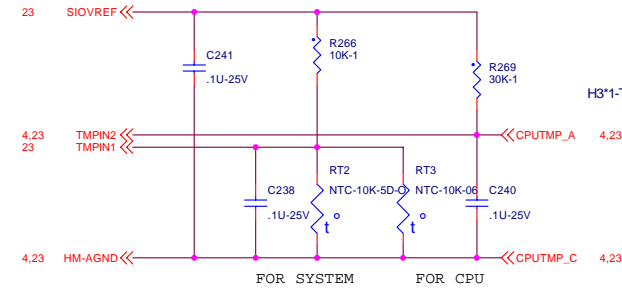


CASEFAN

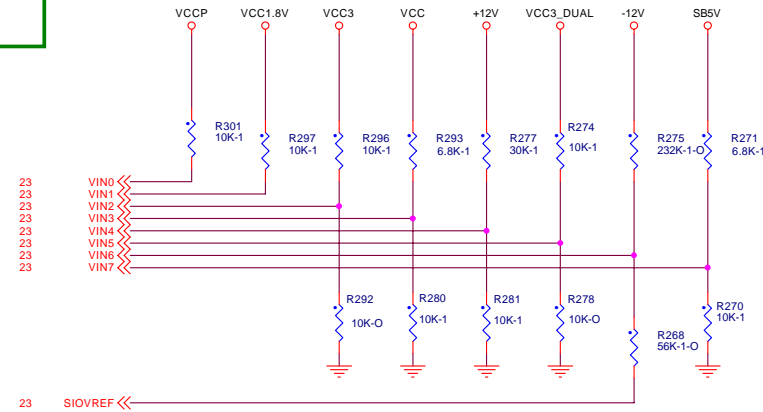


Temperature Monitor

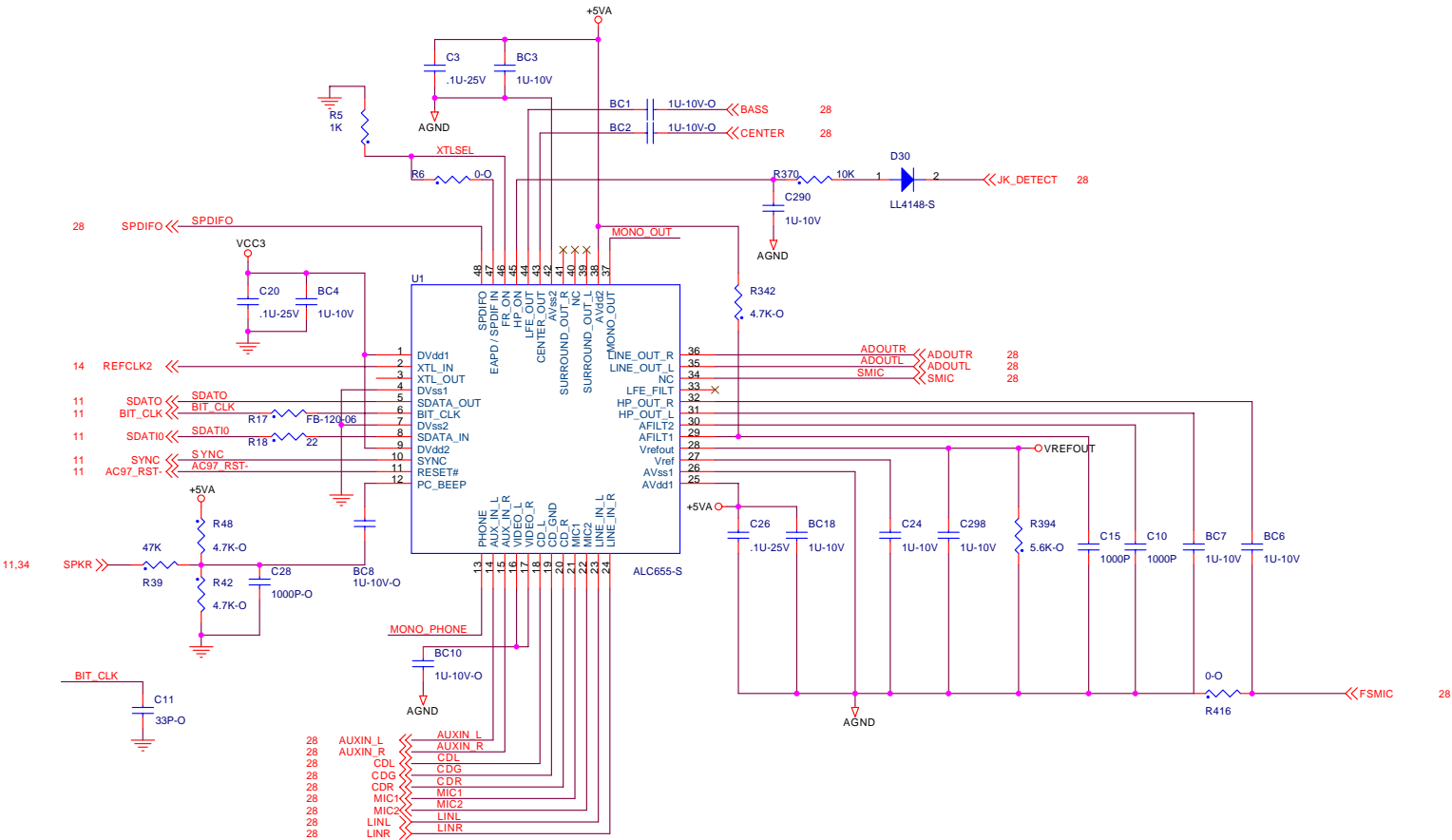
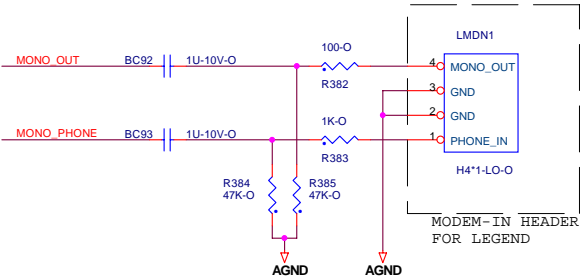
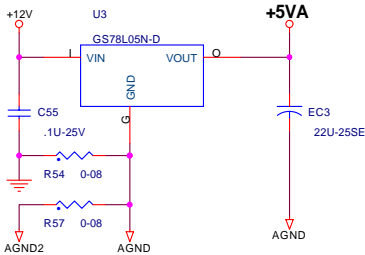
Choosing method of measuring temperature by either thermistor or diode



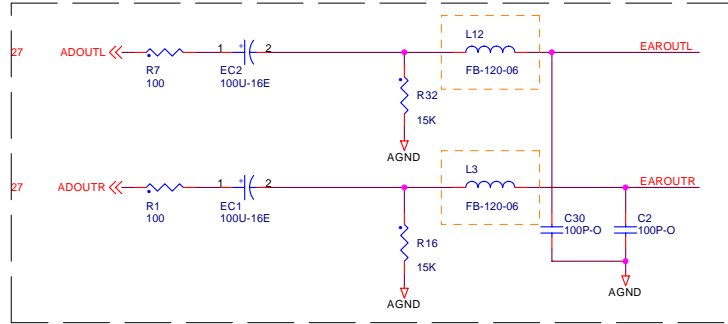
Voltage Monitor



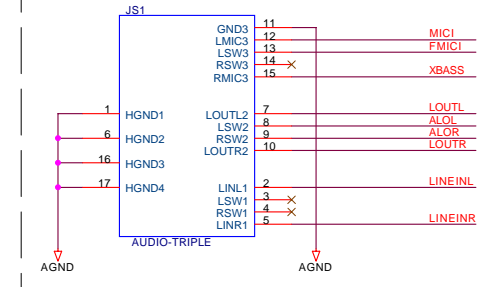
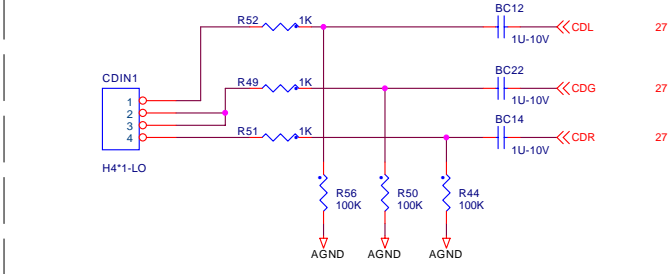
	R2	BC9	BC5	R26	BC9	BC20	R27	L2	BC6	BC7
CMI9738	0	Open	Open	Open	Open	Open	Open	Open	Open	Open
CMI9739A	Open	Open	Open	Open	Open	1U	3K	FB	Open	Open
CMI9760	Open	Open	1U	3K	Open	1U	3K	FB	Open	Open
ALC655	Open	1U	Open	3K	1U	Open	3K	FB	1U	1U



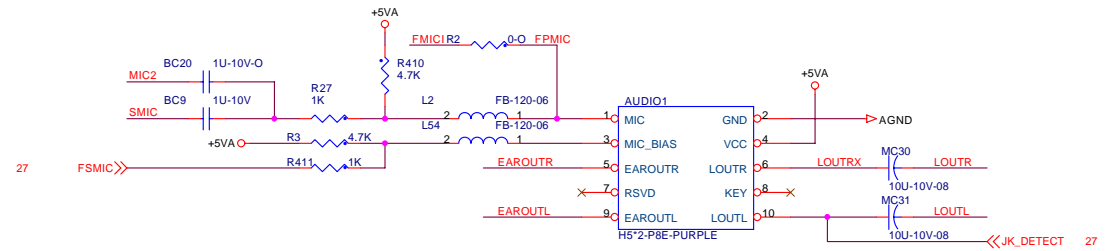
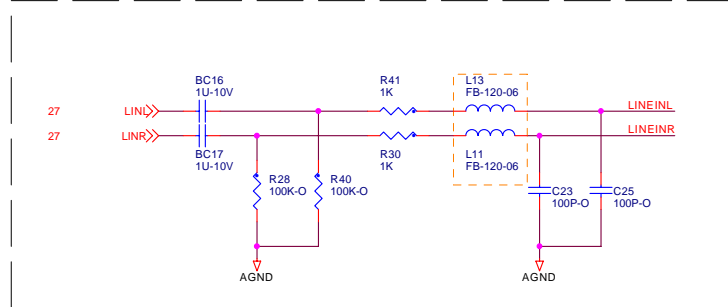
SPEAKER-OUT



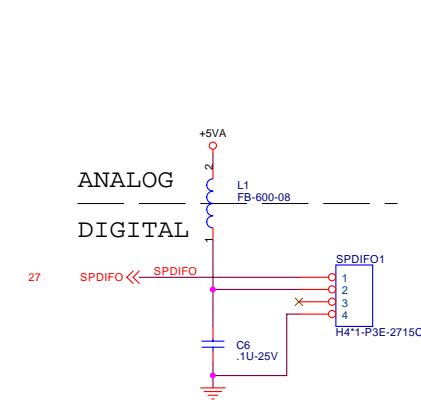
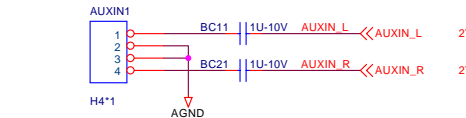
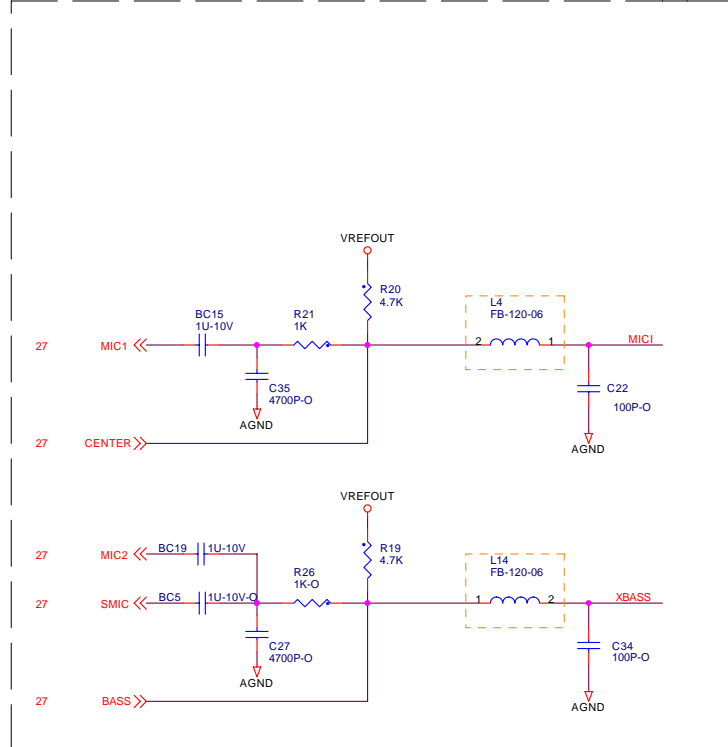
CD-IN

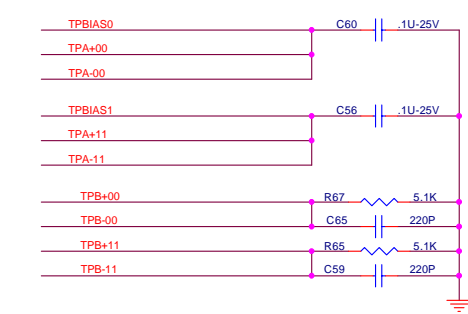
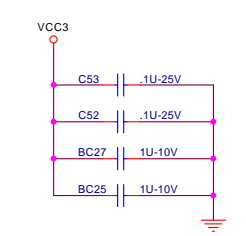
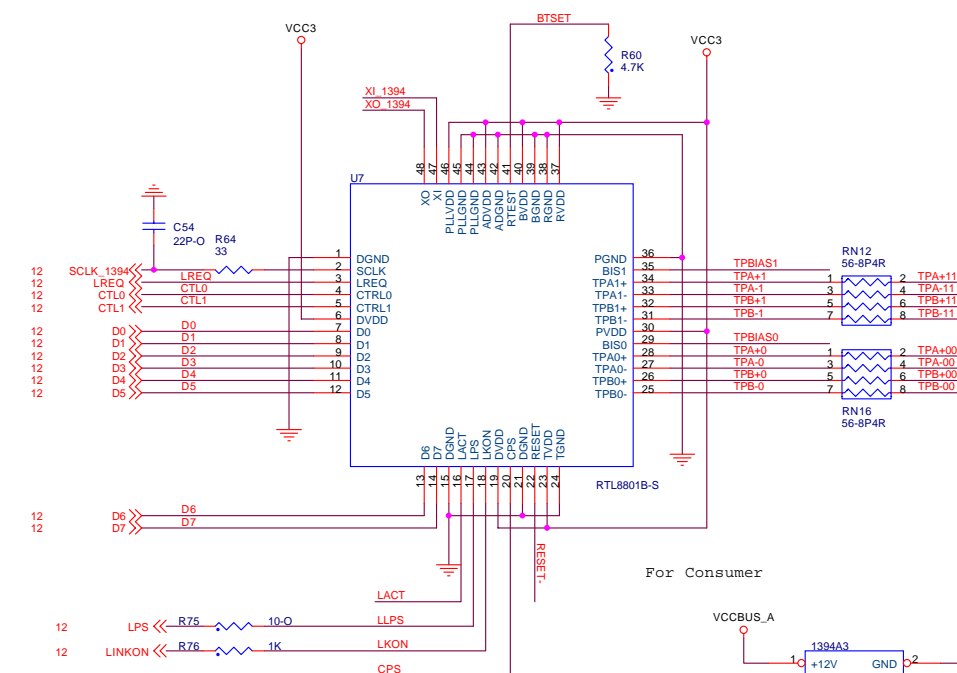
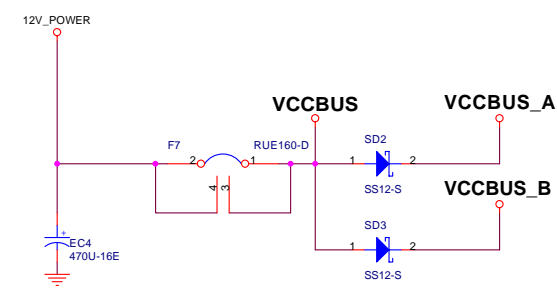
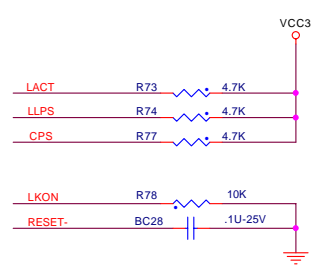
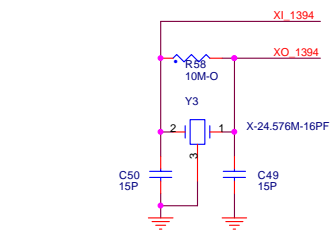


LINE-IN / SURROUND-OUT

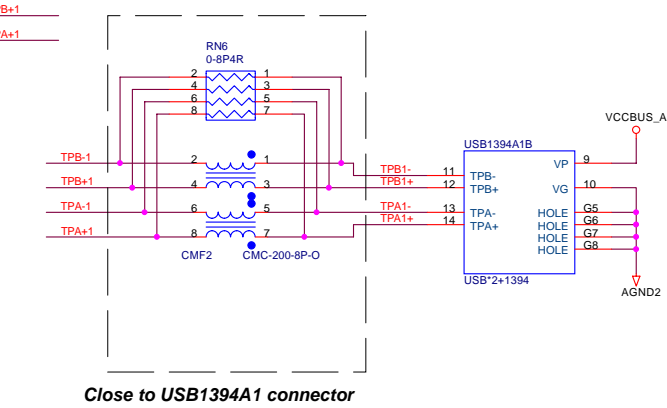
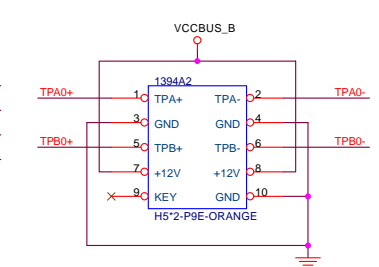
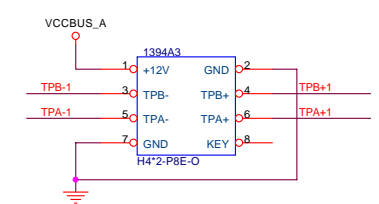


MIC-IN / CENTER-BASS OUT

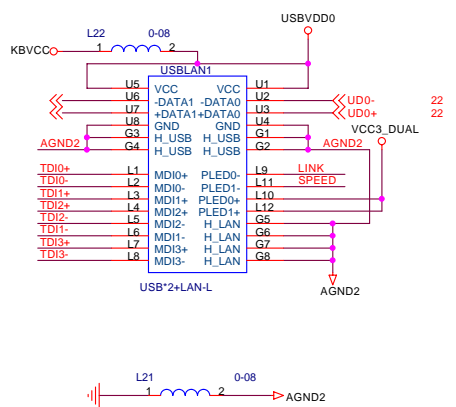
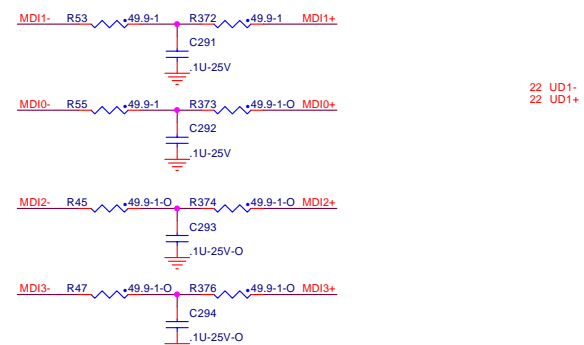
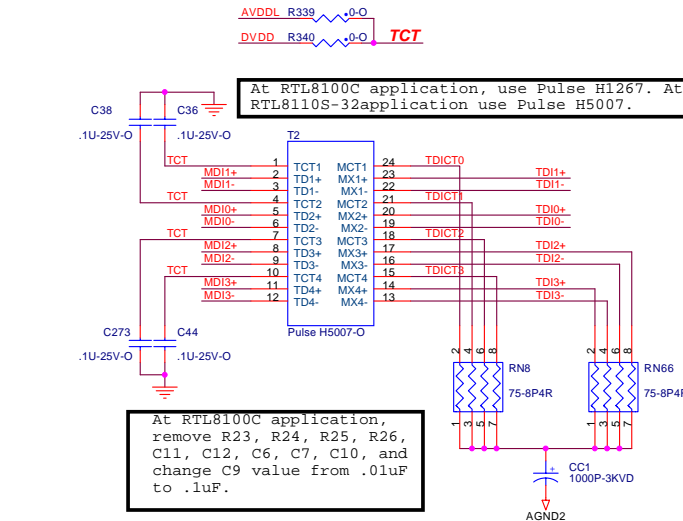
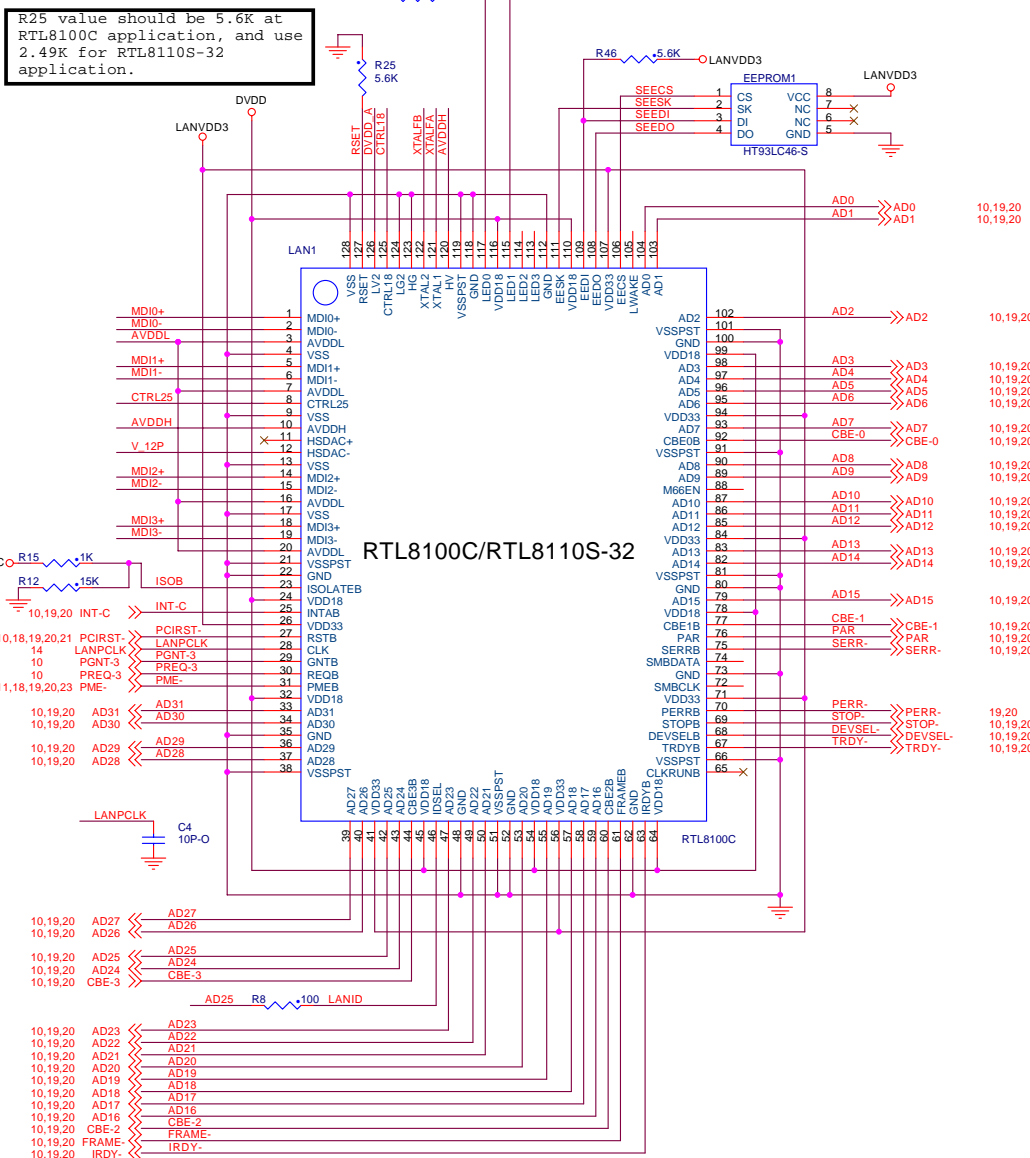
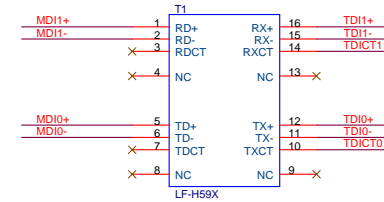
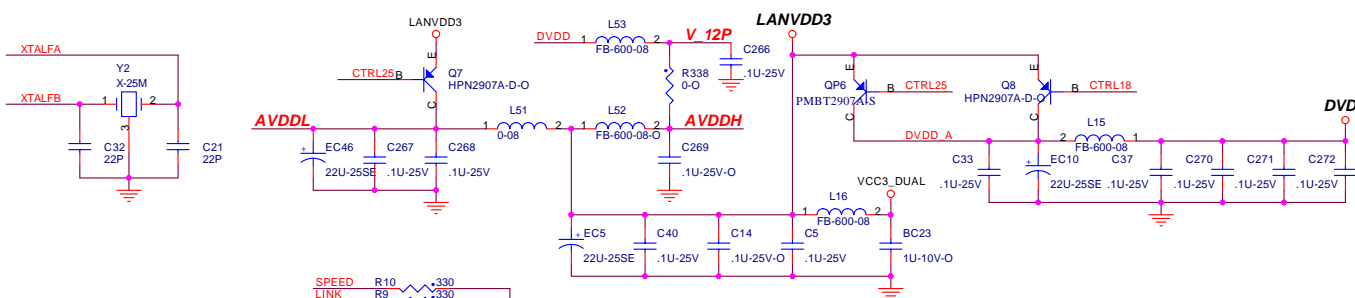




For Consumer



Close to USB1394A1 connector



	8100C	8110S
VDD3	3.3V	3.3V
AVDDH	X	3.3V
AVDDL	3.3V	2.5V
DVDD	2.5V	1.8V
DVDD_A	2.5V	1.8V
V_12P	2.5V	X

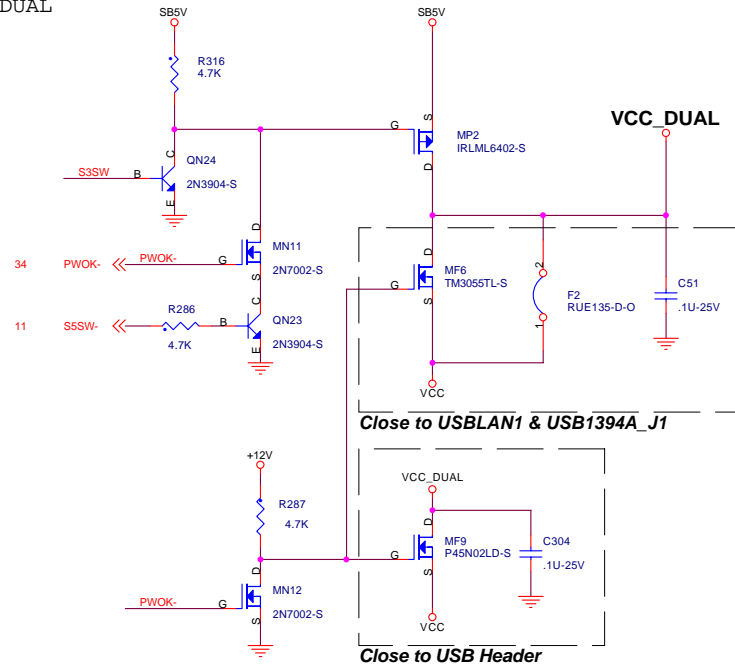
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

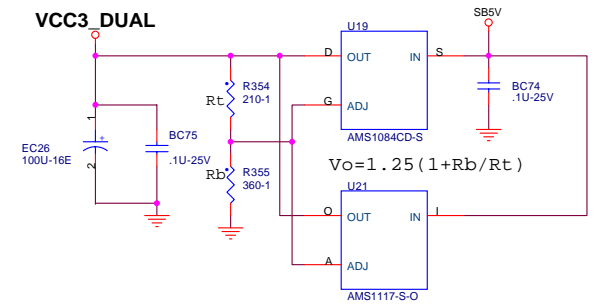
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER.(ADDITIONAL
500mA PER USB PORT)

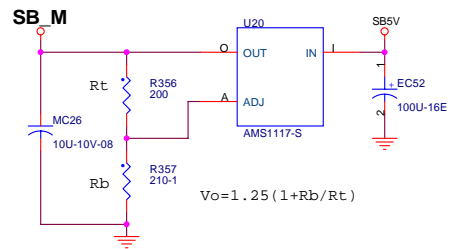
VCC3_DUAL & VCC5_DUAL



VCC3_DUAL

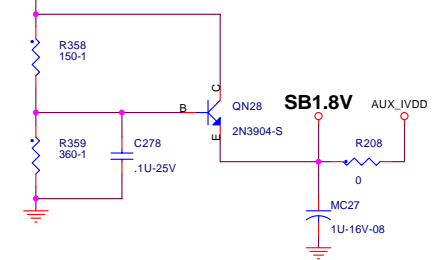


SB_M



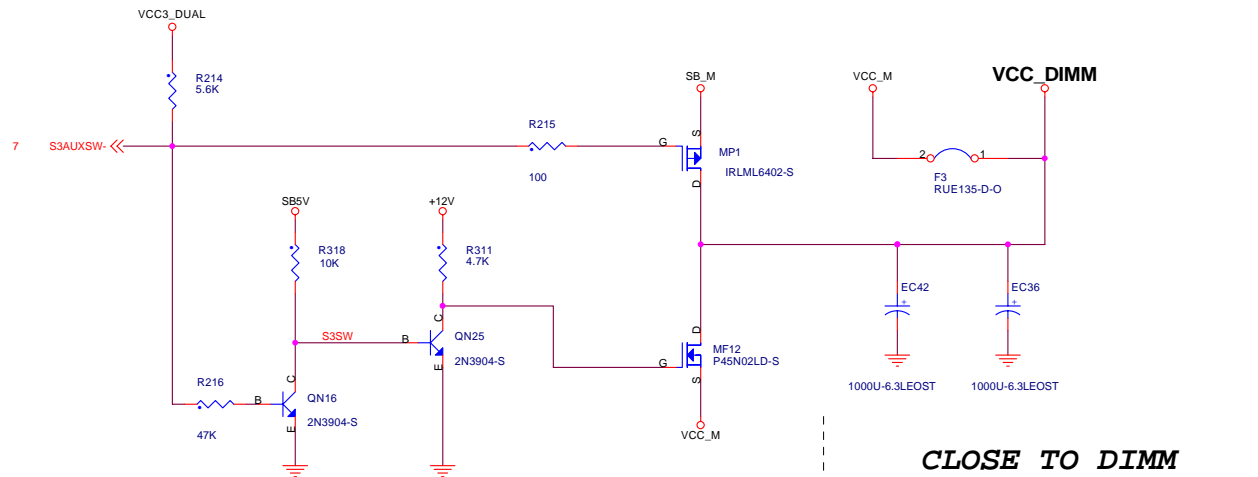
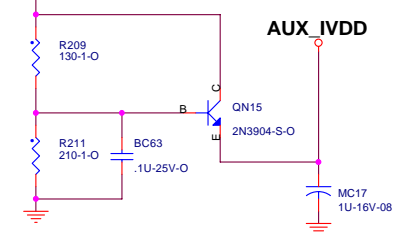
VCC3_DUAL

SB1.8V (For SB) 20mA



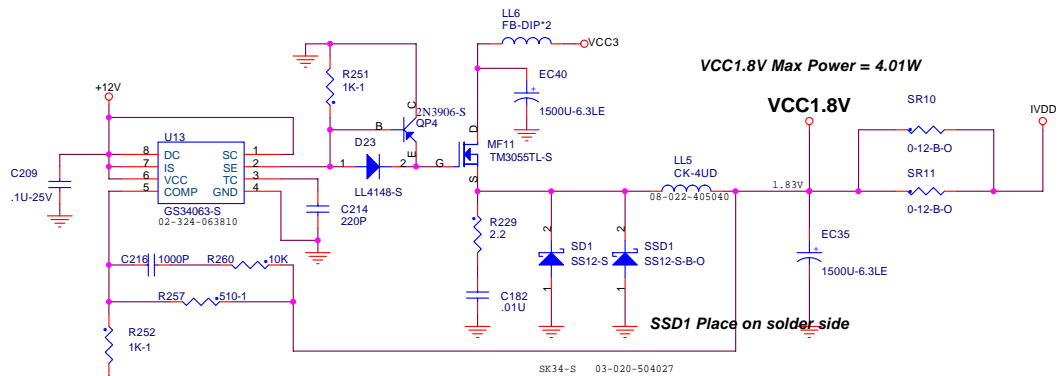
VCC3_DUAL

AUX_IVDD (For NB) 10mA



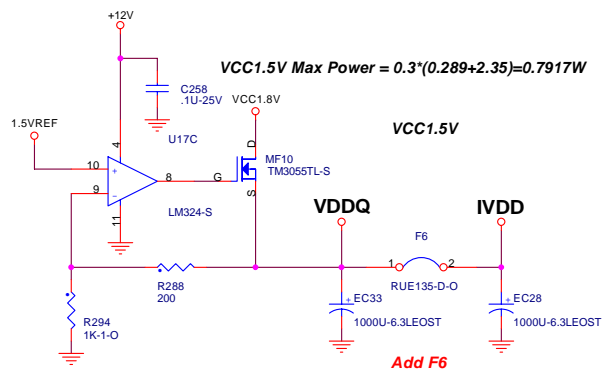
litegroup Computer Systems

Title	SF1/648FX		
Size	Document Number	Dual 5V&3V, STR	
Custom			Rev 1.1
Date	Friday, July 11, 2003	Sheet 31	of 34

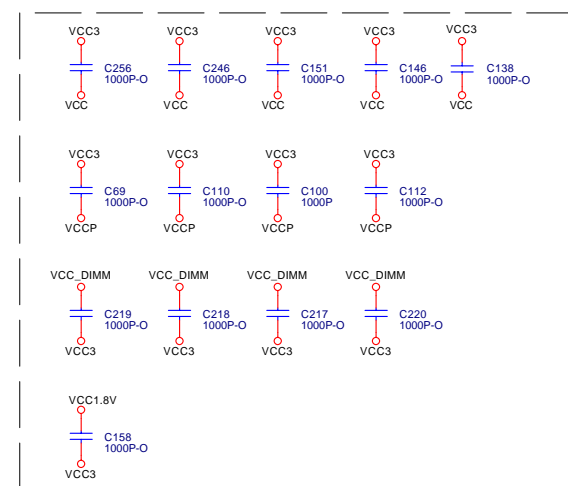
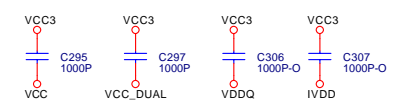
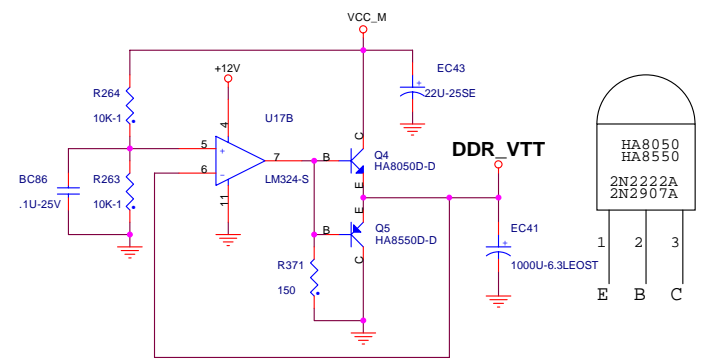
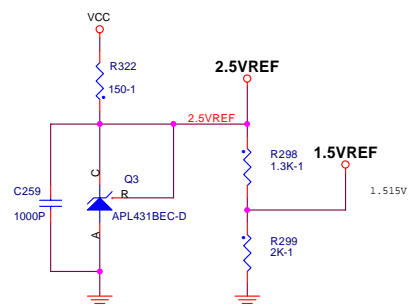


	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

	AUX_IVDD	SBI.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator

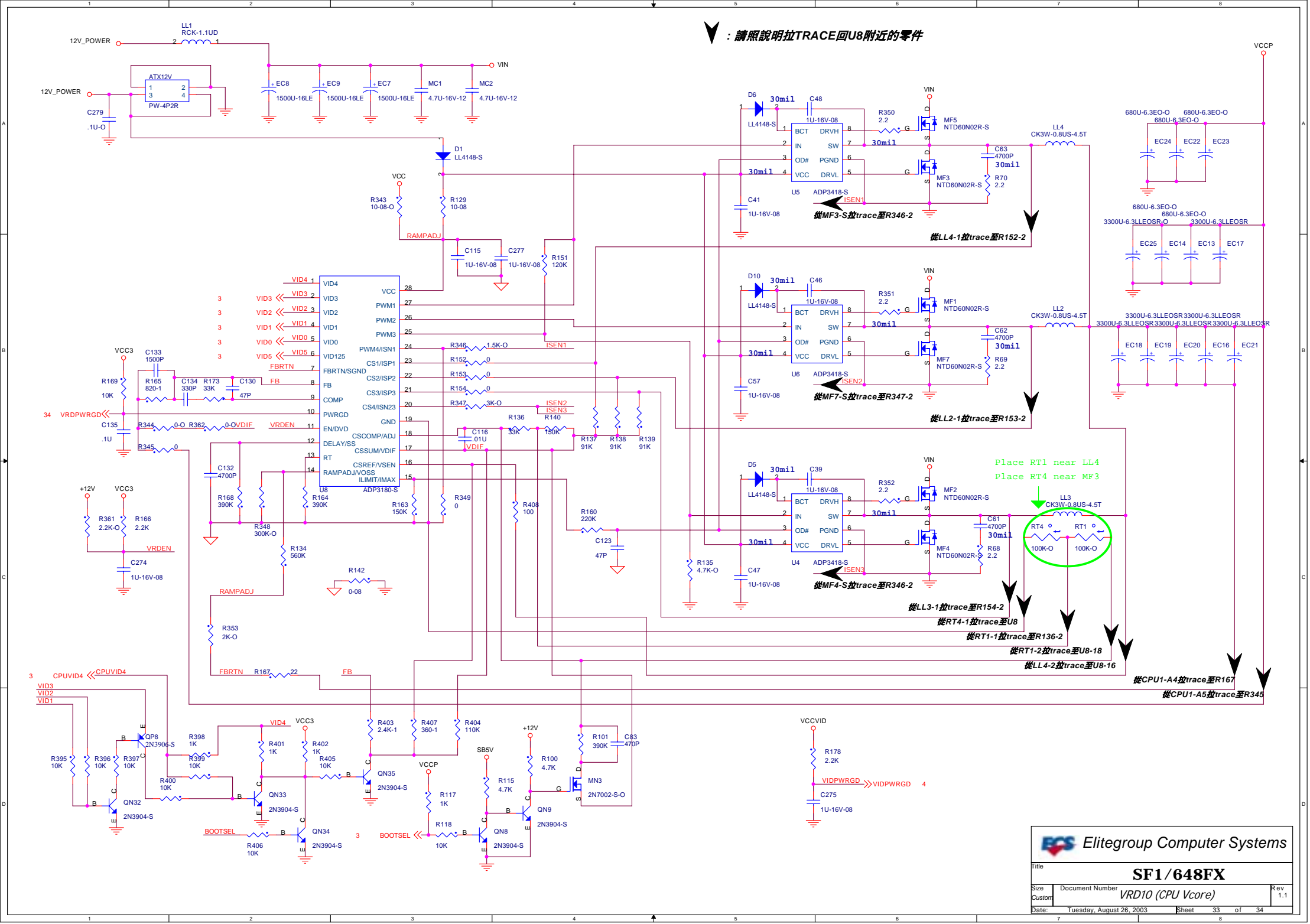


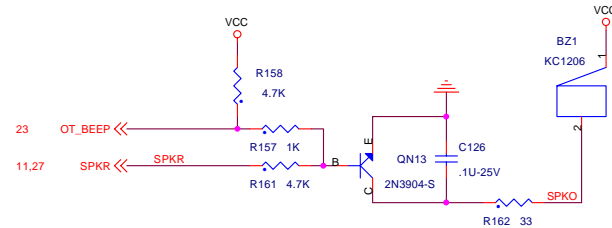
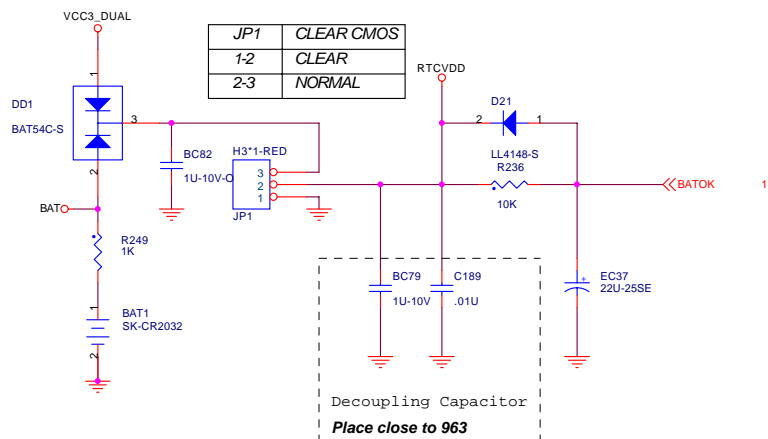
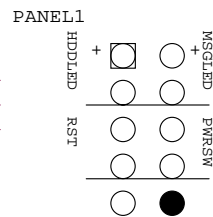
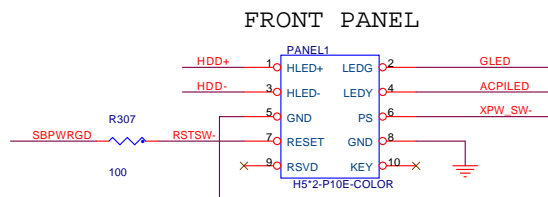
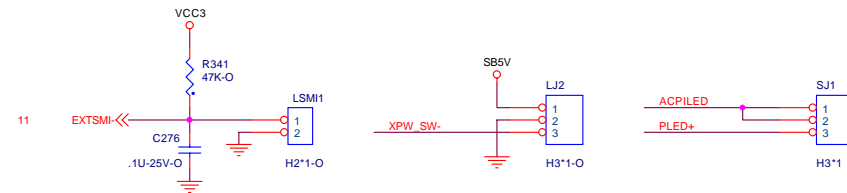
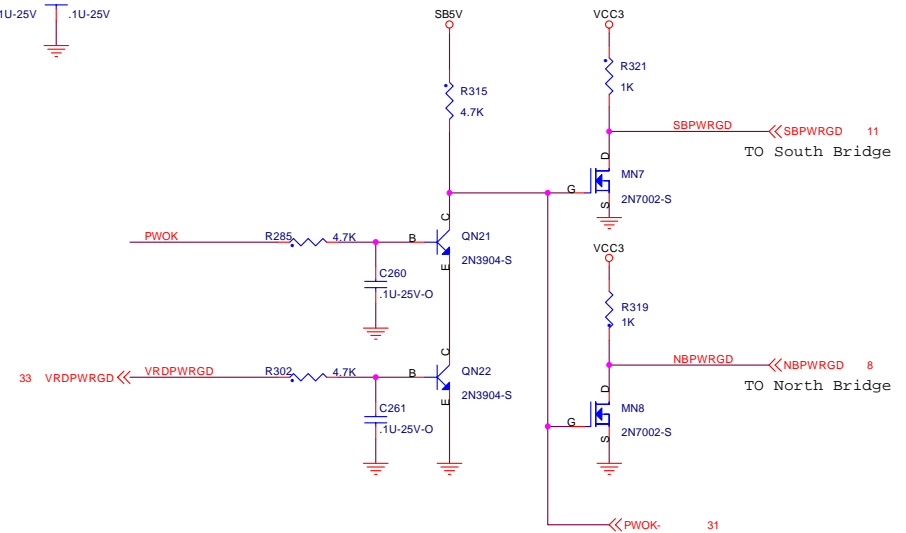
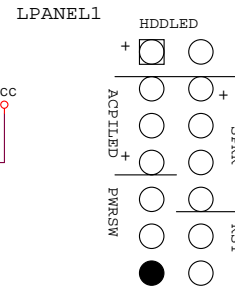
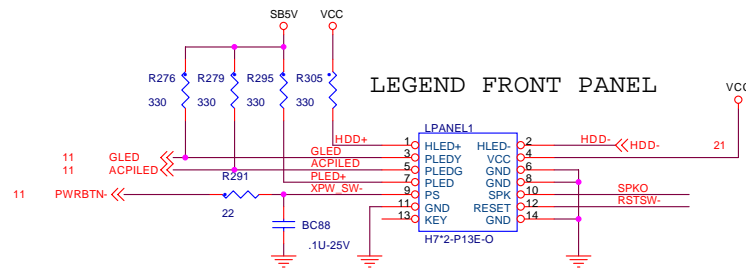
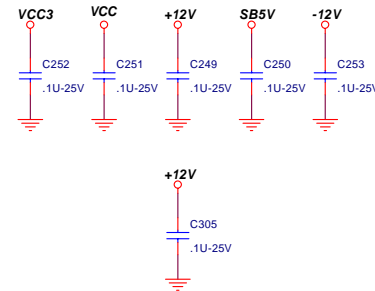
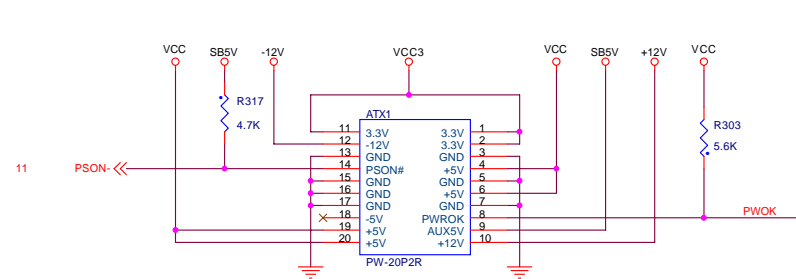
F6	
661LV	SHORT
648	OPEN



平均分佈在POWER PLAN 和 PLAN 之間

DDR_VJ	VCC_M
0	2.54V
1	2.63V





RTC

NOTE!
 1.The RTCVDD is 3V
 2.Decoupling capacitor must be close to 635 RTCVDD pin.
 3.RTC circuit must strictly follow SiS's recommended design
 SiS is not responsible for RTC problems from foreign designs.

